# XD6121/XD6122
# XD6123/XD6124 Series

TOREX

ETR02040-006

☆AEC-Q100 Grade3

Voltage Detector with Watchdog Function and ON/OFF Control

## ■GENERAL DESCRIPTION

The XD6121/XD6122/XD6123/XD6124 series is a group of high-precision, low current consumption voltage detectors with watchdog functions incorporating CMOS process technology. The series consist of a reference voltage source, delay circuit, comparator, and output driver. With the built-in delay circuit, the series do not require any external components to output signals with release delay time. The output type is $V_{DFL}$ low when detected. The EN/ENB pin can control ON and OFF of the watchdog functions. By setting the EN/ENB pin to low or high level, the watchdog function can be OFF while the voltage detector remains operation. Since the EN/ENB pin of the XD6122 and XD6124 series is internally pulled up to the $V_{IN}$ pin or pulled down to the $V_{SS}$ pin, these series can be used with the EN/ENB pin left open when the watchdog functions is used. The detect voltages are 1.6V, 2.2V, 2.3V, 2.4V, 2.9V, 3.0V, 3.1V, 4.4V, 4.5V, 4.6V, using laser trimming technology. Six watchdog timeout periods are available in a range from 50ms to 1.6s. Five release delay times are available in a range from 3.13ms to 400ms.

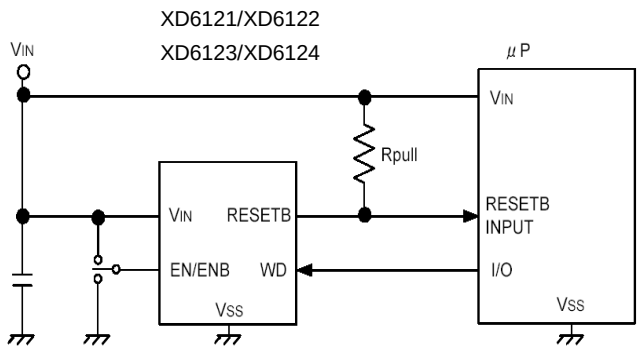
## ■APPLICATIONS

- Microprocessor watchdog monitoring and reset circuits
- Memory battery backup circuits
- System power-on reset circuits
- Power failure detection

## ■FEATURES

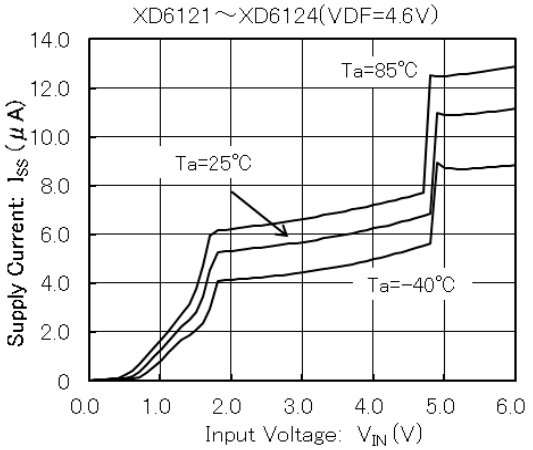
| | |
|---|---|
| **Detect Voltage Range (Standard)** | : 1.6V, 2.2V, 2.3V, 2.4V, 2.9V, 3.0V, 3.1V, 4.4V, 4.5V, 4.6V |
| **Hysteresis Width** | : $V_{DFL}$ x 5% (TYP.) |
| **Operating Voltage Range** | : 1.0V ~ 6.0V |
| **Detect Voltage Temperature Characteristics** | : ±100ppm/°C (TYP.) |
| **Output Configuration** | : N-channel open drain |
| **Watchdog Pin** | : Watchdog input<br>If watchdog input maintains 'H' or 'L' within the watchdog timeout period, a reset signal is output from the RESETB pin. |
| **EN/ENB Pin** | : When the EN/ENB pin voltage is set to low or high level, the watchdog function is forced off. |
| **Release Delay Time** | : 400ms, 200ms, 100ms, 50ms, 3.13ms (TYP.) |
| **Watchdog Timeout Period** | : 1.6s, 800ms, 400ms, 200ms, 100ms, 50ms (TYP.) |
| **Operating Ambient Temperature** | : -40℃~ +85℃ |
| **Package** | : SOT-25 |
| **Environmentally Friendly** | : EU RoHS Compliant, Pb Free |

## ■TYPICAL APPLICATION CIRCUIT



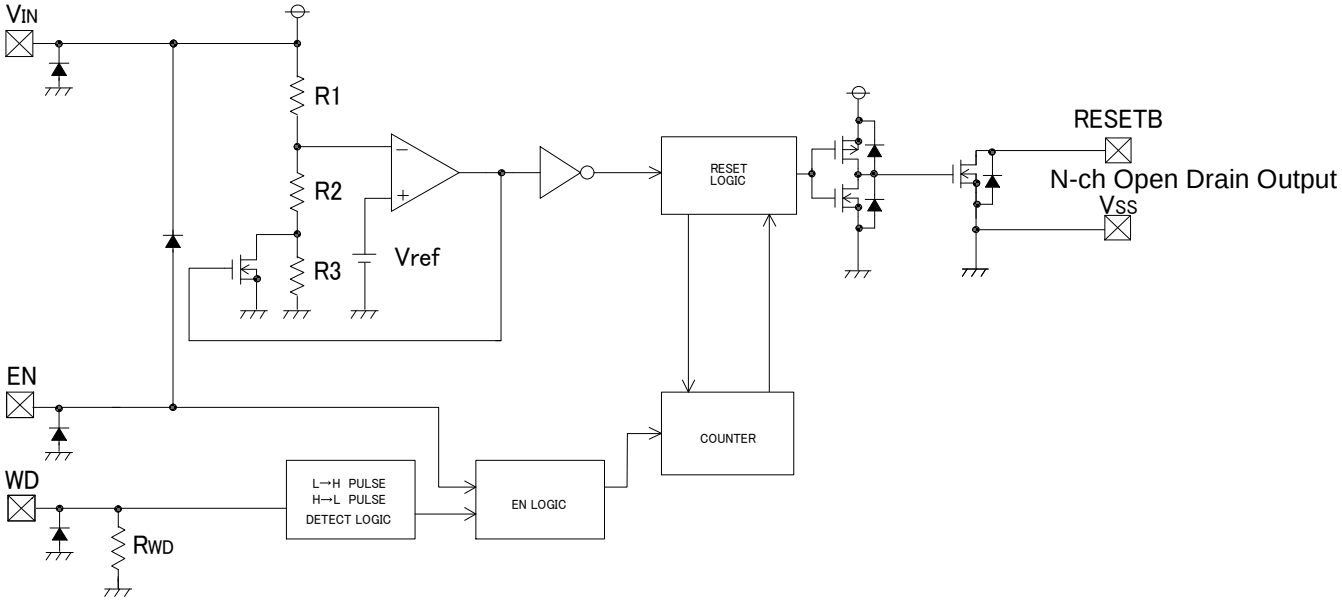

## ■TYPICAL PERFORMANCE CHARACTERISTICS

●Supply Current vs. Input Voltage



# ■BLOCK DIAGRAMS

●XD6121 Series

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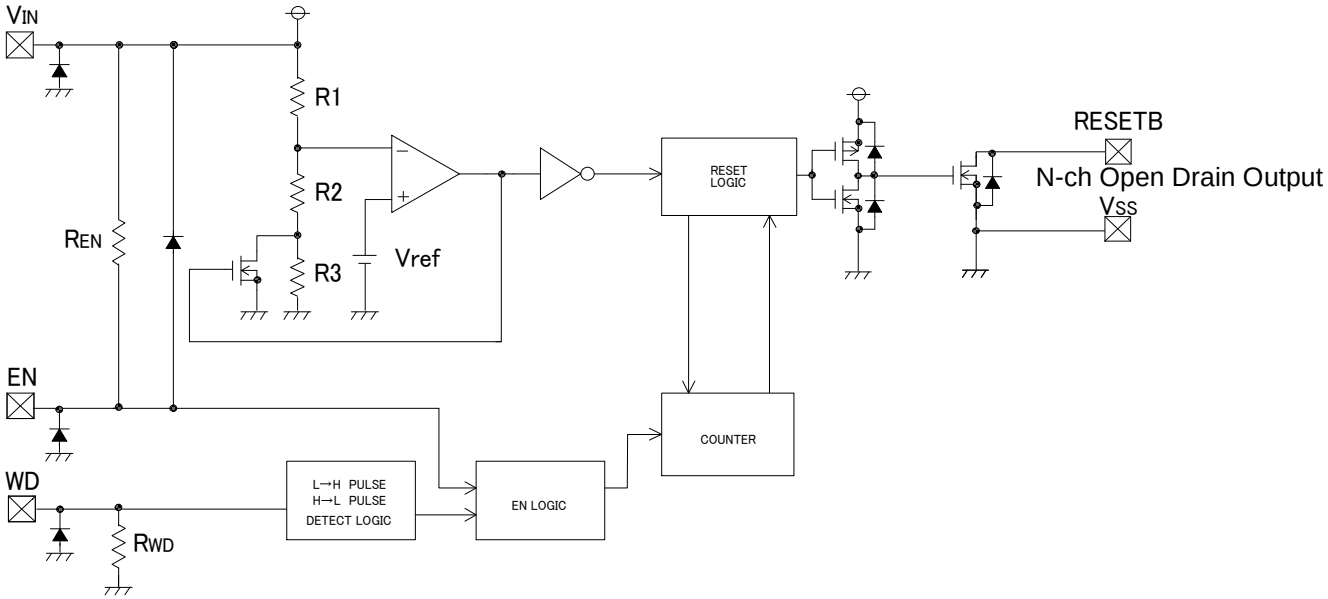
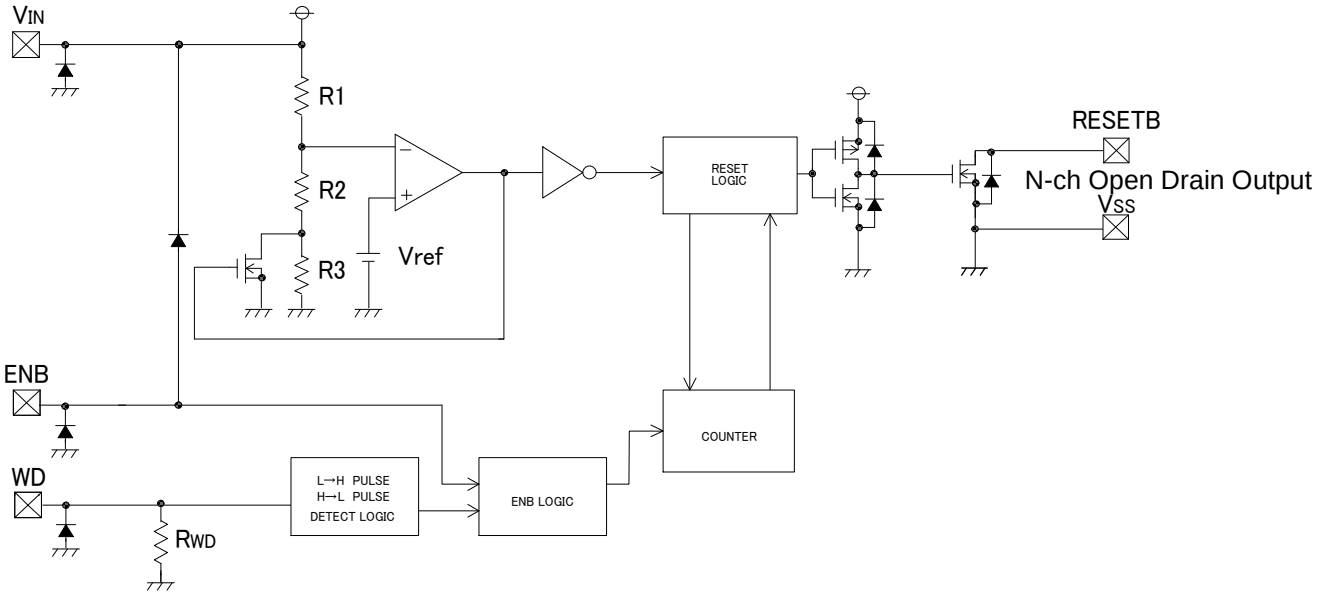
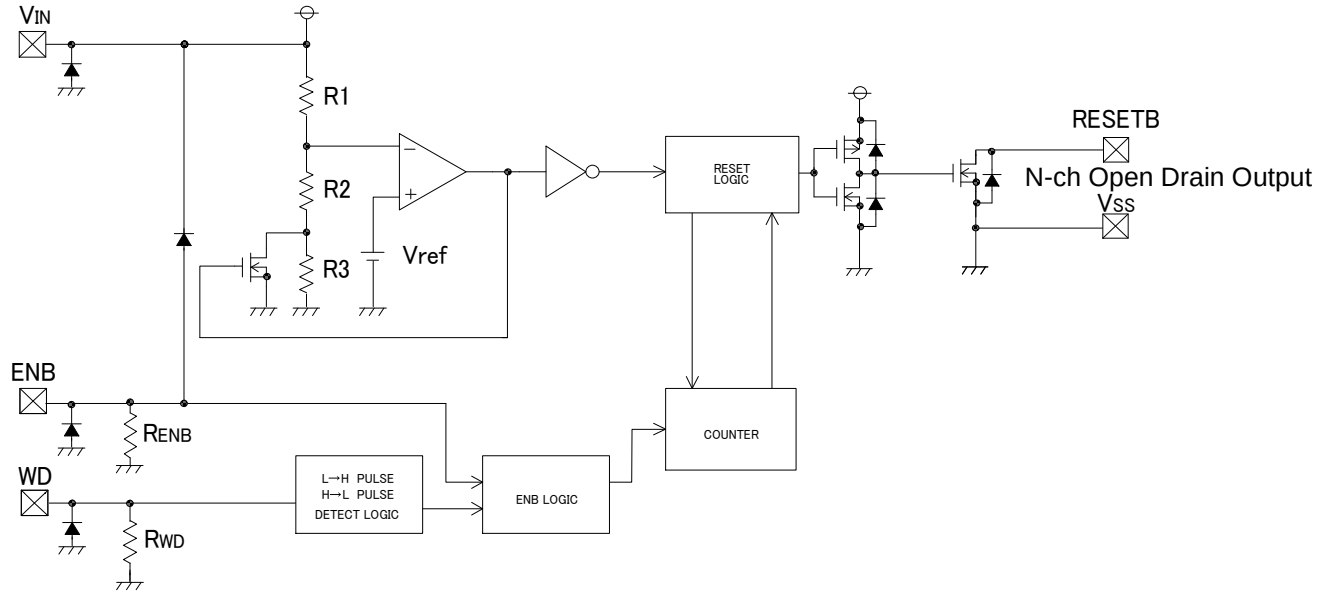


# ■BLOCK DIAGRAMS (Continued)

●XD6123 Series




●XD6124 Series



# ■PRODUCT CLASSIFICATION

## ●Selection Guide

| SERIES | RESET OUTPUT | | HYSTERESIS | EN/ENB PIN FUNCTION | |
|---|---|---|---|---|---|
| | $V_{DFL}$ (RESETB) (*1) | $V_{DFH}$ (RESET) | | EN/ENB Input Logic (*2) | Pull-Up or Down Resistor |
| XD6121 | N-channel open drain | - | Available: $V_{DFL}$ x 5% (TYP.) | EN | With No Pull-Up Resistor |
| XD6122 | N-channel open drain | - | | EN | With Pull-Up Resistor |
| XD6123 | N-channel open drain | - | | ENB | With No Pull-Down Resistor |
| XD6124 | N-channel open drain | - | | ENB | With Pull-Down Resistor |

(*1) The output type of RESETB is set to L level at the time of detection.

(*2) EN input logic: The watchdog function turns on when the EN pin becomes high level.
ENB input logic: The watchdog function turns on when the ENB pin becomes low level.

## ●Ordering Information

XD6121①②③④⑤⑥−⑦(*2): N-channel Open Drain Output (RESETB), EN Pin: No Pull-Up Resistor
XD6122①②③④⑤⑥−⑦(*2): N-channel Open Drain Output (RESETB), EN Pin: Pull-Up Resistor
XD6123①②③④⑤⑥−⑦(*2): N-channel Open Drain Output (RESETB), ENB Pin: No Pull-Down Resistor
XD6124①②③④⑤⑥−⑦(*2): N-channel Open Drain Output (RESETB), ENB Pin: Pull-Down Resistor

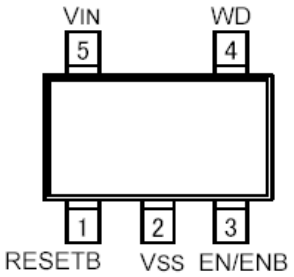
| DESIGNATOR | ITEM | SYMBOL | DESCRIPTION |
|---|---|---|---|
| ① | Release Delay Time(*1) | A | 3.13ms (TYP.) |
| | | C | 50ms (TYP.) |
| | | D | 100ms (TYP.) |
| | | E | 200ms (TYP.) |
| | | F | 400ms (TYP.) |
| ② | Watchdog Timeout Period | 2 | 50ms (TYP.) |
| | | 3 | 100ms (TYP.) |
| | | 4 | 200ms (TYP.) |
| | | 5 | 400ms (TYP.) |
| | | 6 | 1.6s (TYP.) |
| | | 7 | 800ms (TYP.) |
| ③④ | Detect Voltage | 16,22,23,24,29, 30,31,44,45,46(*2) | Detect voltage ex.) 4.5V: ③⇒4, ④⇒5 |
| ⑤⑥−⑦(*3) | Package (Order Unit) | MR-Q | SOT-25 (3,000pcs/Reel) |

(*1) Please set the release delay time shorter than or equal to the watchdog timeout period.
ex.) XD6123F523MR or XD6123F623MR

(*2) For other output voltages, please contact your local Torex sales office or representative. The output voltage optional range is 1.6V to 5.0V.

(*3) The “-Q” suffix denotes “AEC-Q100” and “Halogen and Antimony free” as well as being fully EU RoHS compliant.

## ■PIN CONFIGURATION




SOT-25
(TOP VIEW)

## ■PIN ASSIGNMENT

| PIN NUMBER | PIN NAME | FUNCTIONS |
|---|---|---|
| SOT-25 | | |
| 1 | RESETB | Reset Output |
| 2 | $V_{SS}$ | Ground |
| 3 | EN/ENB | Watchdog ON/OFF Control |
| 4 | WD | Watchdog |
| 5 | $V_{IN}$ | Power Input |

## ■PIN LOGIC CONDITIONS

| PIN NAME | LOGIC | CONDITIONS |
|---|---|---|
| $V_{IN}$ | H | $V_{IN} \geqq V_{DFL}+V_{HYS}$ |
| | L | $V_{IN} \leqq V_{DFL}$ |
| EN/ENB | H | $V_{EN}/V_{ENB} \geqq 1.30V$ |
| | L | $V_{EN}/V_{ENB} \leqq 0.35V$ |
| WD | H | The state maintaining $WD \geqq V_{WDH}$ for more than $t_{WD}$ |
| | L | The state maintaining $WD \leqq V_{WDL}$ for more than $t_{WD}$ |
| | L→H | $V_{WDL} \rightarrow V_{WDH}$, $300ns \leqq t_{WDIN} \leqq t_{WD}$ |
| | H→L | $V_{WDH} \rightarrow V_{WDL}$, $300ns \leqq t_{WDIN} \leqq t_{WD}$ |

NOTE:
$V_{DFL}$: Detect Voltage
$V_{HYS}$: Hysteresis Range
$V_{WDH}$: WD High Level Voltage
$V_{WDL}$: WD Low Level Voltage
$t_{WDIN}$: WD Pulse Width
$t_{WD}$: WD Timeout Period
For the details of each parameter, please see the electrical characteristics.

## ■FUNCTION CHART

| $V_{IN}$ | XD6121/XD6122 | XD6123/XD6124 | $V_{WD}$ | $V_{RESETB}$ (*2) |
|---|---|---|---|---|
| | $V_{EN}$ | $V_{ENB}$ | | |
| H | H | L | H | Repeating detect and release (H→L→H) |
| | | | L | |
| | | | OPEN | |
| | | | L⇔H | H |
| H | L | H | *1 | H |
| L | | L | | L |

NOTE:
*1: Including all logics of the WD ($V_{WD}$=H, L, OPEN, H→L, L→H).
*2: When the $V_{RESETB}$ is High, the circuit is in the release state.
When the $V_{RESETB}$ is Low, the circuit is in the detection state.
*3: $V_{IN}$=L and $V_{EN}$/$V_{ENB}$=H cannot be combined because the rated input voltage of the EN/ENB pin is $V_{SS}$-0.3V to $V_{IN}$+0.3V.
*4: The RESETB pin becomes indefinite operation while 0.35V<$V_{EN}$/$V_{ENB}$<1.3V.
*5: The EN pin of the XD6121 series is not internally pulled up. When using the watchdog function, please drive the $V_{EN}$ pin in high level. The EN pin of the XD6122 series is internally pulled up. The watchdog function can be used even the EN pin left open. The ENB pin of the XD6123 series is not internally pulled down. When using the watchdog function, please drive the $V_{ENB}$ pin in low level. The ENB pin of the XD6124 series is internally pulled up. The watchdog function can be used even the ENB pin left open.

## ■ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | SYMBOL | RATINGS | UNITS |
|---|---|---|---|---|
| Input Voltage | | $V_{IN}$ | -0.3～7.0 | V |
| | | $V_{EN}$/$V_{ENB}$ | -0.3～$V_{IN}$+0.3 or +7.0(*1) | V |
| | | $V_{WD}$ | -0.3～+7.0 | V |
| Output Current | | $I_{RBOUT}$ | 20 | mA |
| Output Voltage | | $V_{RESETB}$ | -0.3～+7.0 | V |
| Power Dissipation (Ta=25℃) | SOT-25 | Pd | 250 | mW |
| | | | 600(40mm x 40mm Standard board) (*2) | |
| | | | 760(JESD51-7 board) (*2) | |
| Operating Ambient Temperature | | Topr | -40 ~ +85 | °C |
| Storage Temperature | | Tstg | -55 ~ +125 | °C |

(*1) The maximum value should be either $V_{IN}$ +0.3 or +7.0 in the lowest.
(*2) The power dissipation figure shown is PCB mounted and is for reference only.
The mounting condition is please refer to PACKAGING INFORMATION.

# ■ELECTRICAL CHARACTERISTICS

Ta=25 °C

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---|---|---|---|---|---|---|---|
| Detect Voltage | $V_{DFL}$ | $V_{EN}=V_{SS}$ | $V_{DFL(T)}$ × 0.98 | $V_{DFL(T)}$ | $V_{DFL(T)}$× 1.02 | V | ① |
| | | -40°C ≦ Topr ≦85 °C | $V_{DFL(T)}$ × 0.96 | $V_{DFL(T)}$ | $V_{DFL(T)}$× 1.04 | | |
| Hysteresis Width | $V_{HYS}$ | $V_{EN}=V_{SS}$ | $V_{DFL}$ × 0.02 | $V_{DFL}$ × 0.05 | $V_{DFL}$ × 0.08 | V | ① |
| | | -40°C ≦ Topr ≦85 °C | $V_{DFL}$ × 0.01 | $V_{DFL}$ × 0.05 | $V_{DFL}$ × 0.08 | | |
| Supply Current (*1) | $I_{SS}$ | WD=OPEN, $V_{IN}=V_{DFL(T)}$×0.9V | - | 5 | 11 | μA | ① |
| | | -40°C ≦ Topr ≦85 °C | - | - | 20 | | |
| | | WD=OPEN, $V_{IN}=V_{DFL(T)}$×1.1V | - | 10 | 16 | | |
| | | -40°C ≦ Topr ≦85 °C | - | - | 28 | | |
| | | WD=OPEN, $V_{IN}$=6.0V | - | 12 | 18 | | |
| | | -40°C ≦ Topr ≦85 °C | - | - | 35 | | |
| Operating Voltage | $V_{IN}$ | -40°C ≦ Topr ≦85 °C | 1.0 | - | 6.0 | V | ① |
| Output Current | $I_{RBOUT}$ | N-ch. $V_{DS}$=0.5V, $V_{IN}$=1.0V | 0.15 | 0.5 | - | mA | ③ |
| | | $V_{IN}$=2.0V ($V_{DFL(T)}$> 2.0V) | 2.0 | 2.5 | - | | |
| | | $V_{IN}$=3.0V ($V_{DFL(T)}$ >3.0V) | 3.0 | 3.5 | - | | |
| | | $V_{IN}$=4.0V ($V_{DFL(T)}$ >4.0V) | 3.5 | 4.0 | - | | |
| Release Delay Time ($V_{DFL}$≦1.8V) | $t_{DR}$ | Time until $V_{IN}$ is increased from 1.0V to 2.0V and attains to the release time level, and the Reset output pin releases. | 2.00 | 3.13 | 5.00 | ms | ④ |
| | | | 37 | 50 | 63 | | |
| | | | 75 | 100 | 125 | | |
| | | | 150 | 200 | 250 | | |
| | | | 300 | 400 | 500 | | |
| Release Delay Time ($V_{DFL}$≧1.9V) | $t_{DR}$ | Time until $V_{IN}$ is increased from 1.0V to ($V_{DFL}$ x 1.1V) and attains to the release time level, and the Reset output pin releases. | 2.00 | 3.13 | 5.00 | ms | ④ |
| | | | 37 | 50 | 63 | | |
| | | | 75 | 100 | 125 | | |
| | | | 150 | 200 | 250 | | |
| | | | 300 | 400 | 500 | | |
| Detect Delay Time | $t_{DF}$ | Time until $V_{IN}$ is decreased from 6.0V to 1.0V and attains to the detect voltage level, and the Reset output pin detects while the WD pin left open. | - | 5.5 | 33 | μs | ④ |
| $V_{DFL}$ Leakage Current | $I_{LEAK}$ | $V_{IN}$=6.0V, $V_{RESETB}$=6.0V | - | 0.01 | 0.1 | μA | ③ |
| Watchdog Timeout Period ($V_{DFL}$≦1.8V) | $t_{WD}$ | Time until $V_{IN}$ increases form 1.0V to 2.0V and the Reset output pin is released to go into the detection state. (WD=OPEN) | 37 | 50 | 63 | ms | ⑤ |
| | | | 75 | 100 | 125 | | |
| | | | 150 | 200 | 250 | | |
| | | | 300 | 400 | 500 | | |
| | | | 600 | 800 | 1000 | | |
| | | | 1200 | 1600 | 2000 | | |
| Watchdog Timeout Period ($V_{DFL}$≧1.9V) | $t_{WD}$ | Time until $V_{IN}$ increases from 1.0V to ($V_{DFL}$X1.1V) and the Reset output pin is released to go into the detection state. (WD=OPEN) | 37 | 50 | 63 | ms | ⑤ |
| | | | 75 | 100 | 125 | | |
| | | | 150 | 200 | 250 | | |
| | | | 300 | 400 | 500 | | |
| | | | 600 | 800 | 1000 | | |
| | | | 1200 | 1600 | 2000 | | |

## ■ELECTRICAL CHARACTERISTICS (Continued)

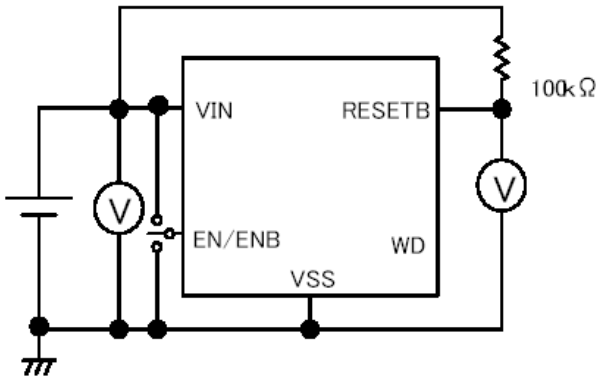
Ta=25 °C

| PARAMETER | SYMBOL | CONDITIONS | | MIN. | TYP. | MAX. | UNITS | CIRCUIT |
|---|---|---|---|---|---|---|---|---|
| Watchdog Minimum Pulse Width | $t_{WDIN}$ | $V_{IN}$=6.0V, Apply pulse from 6.0V to 0V to the WD pin. | | 300 | - | - | ns | ⑥ |
| Watchdog High Level Voltage | $V_{WDH}$ | $V_{IN}=V_{DF}L$ x 1.1V ~ 6.0V | -40°C ≦ Topr ≦ 85 °C | $V_{IN}$ x 0.7 | - | 6 | V | ⑥ |
| Watchdog Low Level Voltage | $V_{WDL}$ | $V_{IN}=V_{DFL}$ x 1.1V ~ 6.0V | -40°C ≦ Topr ≦ 85 °C | 0 | - | $V_{IN}$ x 0.3 | V | ⑥ |
| Watchdog Pull-down Resistance | $R_{WD}$ | $V_{WD}$=6V, $R_{WD}=V_{WD}/I_{WD}$ | | 300 | 600 | 900 | kΩ | ⑦ |
| EN/ENB High Level Voltage | $V_{ENH}/V_{ENBH}$ | $V_{IN}=V_{DFL}$ x 1.1V ~ 6.0V | -40°C ≦ Topr ≦ 85 °C | 1.3 | - | $V_{IN}$ | V | ⑧ |
| EN/ENB Low Level Voltage | $V_{ENL}/V_{ENBL}$ | $V_{IN}=V_{DFL}$ x 1.1V ~ 6.0V | -40°C ≦ Topr ≦ 85 °C | 0 | - | 0.35 | V | ⑧ |
| EN Pull-up Resistance (*2) | $R_{EN}$ | $V_{IN}$=6.0V, $V_{EN}$=0V, $R_{EN}=V_{IN}/I_{EN}$ | | 1.0 | 1.6 | 2.4 | MΩ | ⑨ |
| ENB Pull-down Resistance (*3) | $R_{ENB}$ | $V_{IN}$=6.0V, $V_{ENB}$=6V, $R_{ENB}=V_{ENB}/I_{ENB}$ | | | | | | |

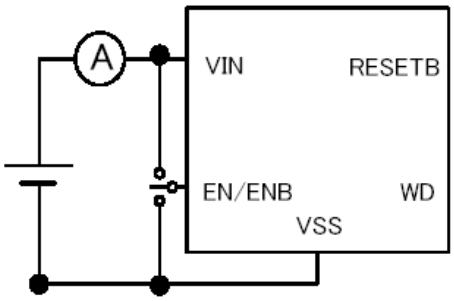
NOTE:
* In case where no EN/ENB pin's condition written in the test condition field, $V_{EN}=V_{IN}$ and $V_{ENB}=V_{SS}$.
** $V_{DFL(T)}$ =Setting detect voltage value
*** The values for -40°C≦Ta≦85°C are designed values.
(*1) The condition when the watchdog pin is ON.
The EN/ENB pin is CMOS input. For the XD6122 (pull-up resistor) and XD6124 (pull-down resistor), supply current increases in the following values when the watchdog function is OFF.
XD6122 Series：（$V_{IN}$-$V_{EHL}$）/1.6MΩ（TYP.）
XD6124 Series：$V_{EHBH}$/1.6MΩ（TYP.）
(*2) For the XD6122 series only.
(*3) For the XD6124 series only.

## ■TEST CIRCUITS

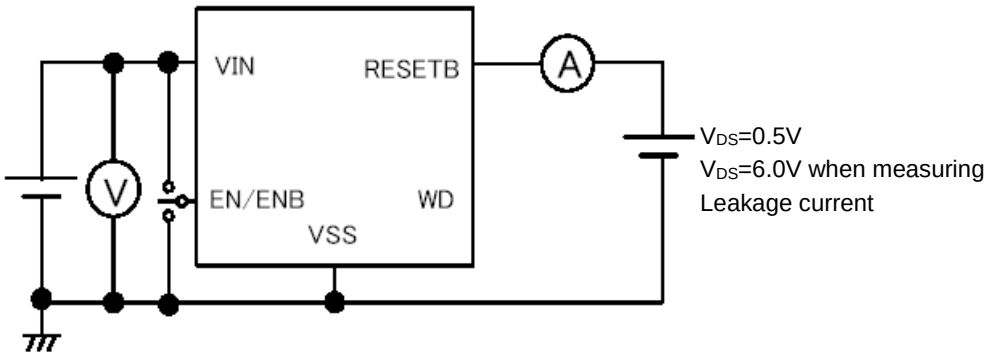
Circuit ①




Circuit ②

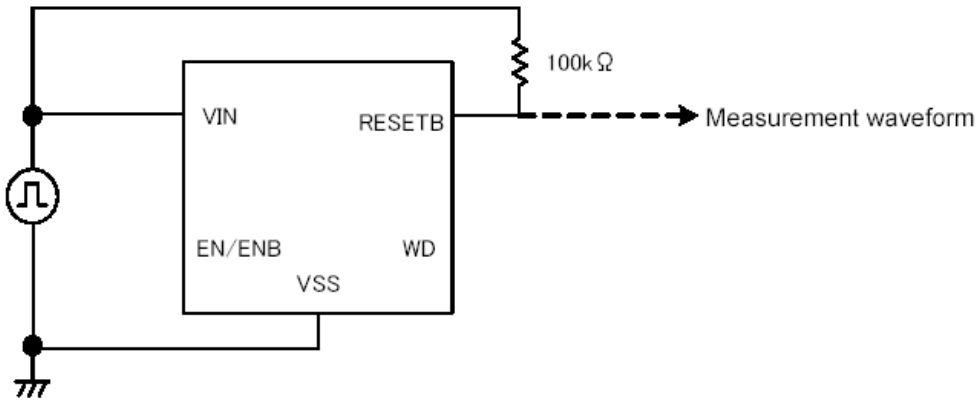



Circuit ③

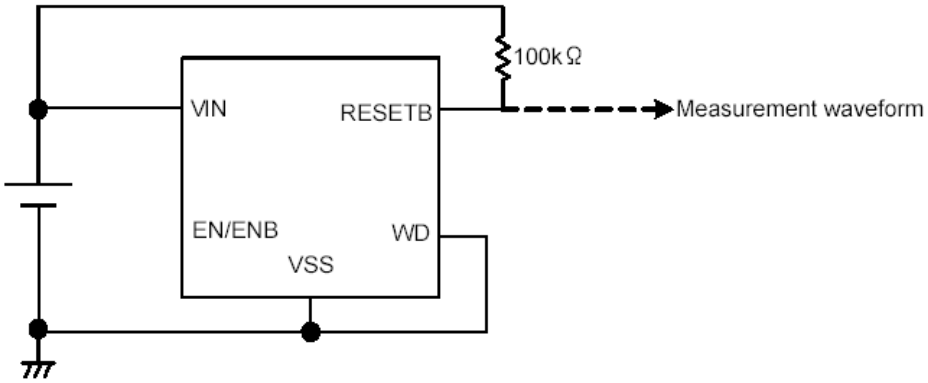


## ■TEST CIRCUITS (Continued)

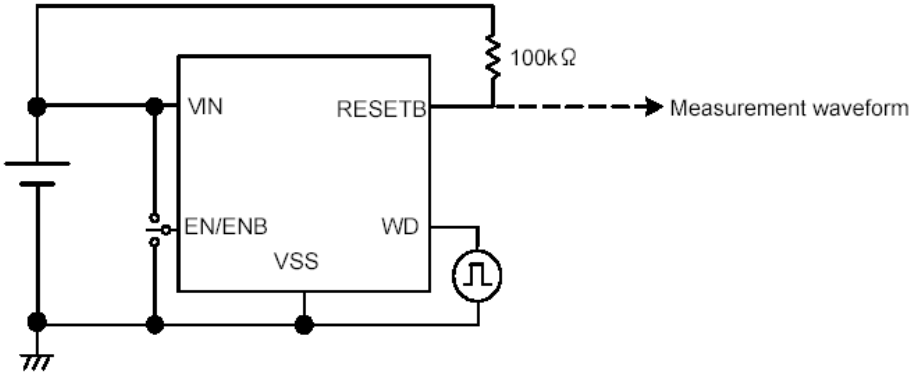
Circuit ④

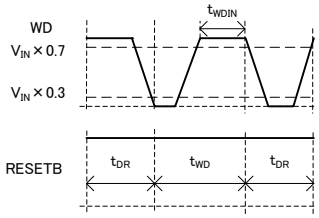



Circuit ⑤



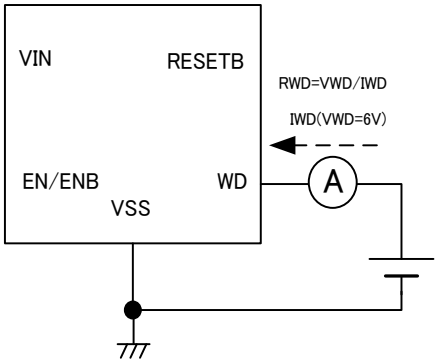

Circuit ⑥



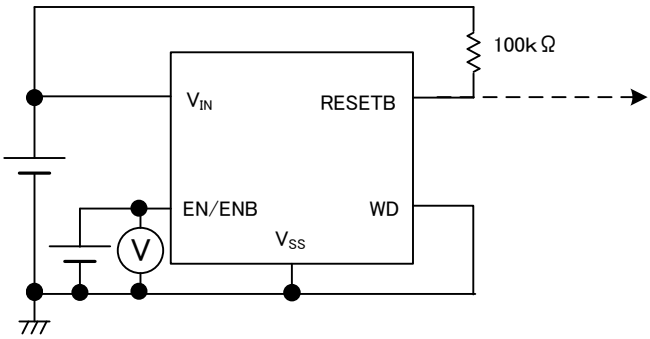



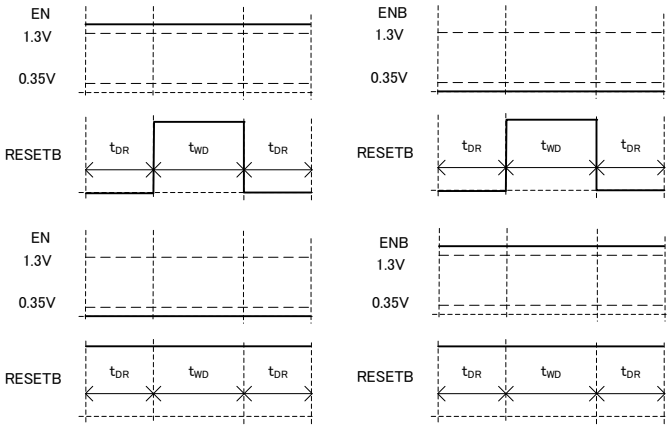
## ■TEST CIRCUITS (Continued)

Circuit ⑦



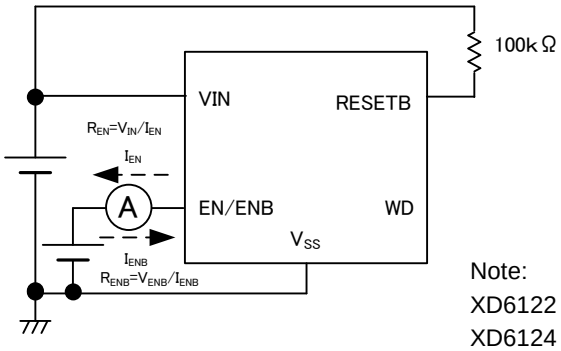

Circuit ⑧




Note: The above reference is about the EN/ENB logic operation.

Circuit ⑨




Note:
XD6122 series has EN pin,
XD6124 Series has ENB pin.

# ■OPERATIONAL EXPLANATION

The XD6121/6122/6123/6124 series compare, using the error amplifier, the voltage of the internal voltage reference source with the voltage divided by R1, R2 and R3 connected to the $V_{IN}$ pin. The resulting output signal from the error amplifier activates the watchdog logic, delay circuit and the output driver. When the $V_{IN}$ pin voltage gradually falls and finally reaches the detect voltage, the RESETB pin output goes from high to low in the case of the $V_{DFL}$ type ICs.

**<RESETB / RESET Pin Output Signal>**

* $V_{DFL}$ (RESETB) type - output signal: Low when detected.

The RESETB pin output goes from high to low whenever the $V_{IN}$ pin voltage falls below the detect voltage. The RESETB pin remains low for the release delay time ($t_{DR}$) after the $V_{IN}$ pin voltage reaches the release voltage. If neither rising nor falling signals are applied to the WD pin within the watchdog timeout period, the RESETB pin output remains low for the release delay time ($t_{DR}$), and thereafter the RESET pin outputs high level signal.

**<Hysteresis>**

When the internal comparator output is high, the NMOS transistor connected in parallel to R3 is turned ON, activating the hysteresis circuit. The difference between the release and detect voltages represents the hysteresis width, as shown by the following calculations:

*$V_{DFL}$ (detect voltage) = (R1+R2+R3) x Vref / (R2+R3)*
*$V_{DR}$ (release voltage) = (R1+R2) x Vref / (R2)*
*$V_{HYS}$ (hysteresis width) =$V_{DR}$-$V_{DFL}$ (V)*
*$V_{DR}$ > $V_{DFL}$*

* Please refer to the block diagrams for R1, R2, R3 and Vref.
* Hysteresis width is selectable from $V_{DFL}$ x 0.05V (TYP.).

**<Watchdog (WD) Pin>**

The series use a watchdog timer to detect malfunction or “runaway” of the microprocessor. If neither rising nor falling signals are applied from the microprocessor within the watchdog timeout period, the RESETB pin output maintains the detection state for the release delay time ($t_{DR}$), and thereafter the RESETB pin outputs low to high signal. The watchdog pin is pulled down to the $V_{SS}$ internally. When the watchdog pin is not connected, A reset signal comes out after the watchdog timeout period. Six watchdog timeout period settings ($t_{WD}$) are available in 1.6s, 800ms, 400ms, 200ms, 100ms, and 50ms.

**<EN Pin>**

In case where the watchdog function is not used, When the EN pin input driven to low level, only the watchdog function is forced off while the detect voltage circuit remains operation. For using the watchdog function, the EN pin should be used in high level. Even after the input voltage and the EN pin voltage are driven back high, the RESETB pin output maintains the detection state for the release delay time ($T_{DR}$). (Refer to the TIMING CHART 1-①.) The watchdog function recovers immediately when the input voltage becomes higher than the release voltage and the EN pin voltage driven from low to high level. (Refer to the TIMING CHART 1-②.) A diode, which is an input protection element, is connected between the EN pin and $V_{IN}$ pin. Therefore, if the EN pin is applied voltage that exceeds $V_{IN}$, the current will flow to $V_{IN}$ through the diode. For avoiding any damage to the IC, please use this IC within the stated maximum ratings ($V_{SS}$ -0.3 ~ $V_{IN}$ +0.3) on the EN pin.

**<ENB Pin>**

In case where the watchdog function is not used, when the ENB pin input driven to high level, only the watchdog function is forced off while the detect voltage circuit remains operation. For using the watchdog function, the ENB pin should be used in low level. Even after the input voltage and the ENB pin voltage are driven back low, the RESETB pin output maintains the detection state for the release delay time ($t_{DR}$). (Refer to the TIMING CHART 2-①.) The watchdog function recovers immediately when the input voltage becomes higher than the release voltage and the ENB pin voltage driven from high to low level. (Refer to the TIMING CHART 2-②.) A diode, which is an input protection element, is connected between the ENB pin and $V_{IN}$ pin. Therefore, if the ENB pin is applied voltage that exceeds $V_{IN}$, the current will flow to $V_{IN}$ through the diode. For avoiding any damage to the IC, please use this IC within the stated maximum ratings ($V_{SS}$ -0.3 ~ $V_{IN}$ +0.3) on the ENB pin.

**<Release Delay Time>**

Release delay time ($t_{DR}$) is the time that elapses from when the $V_{IN}$ pin reaches the release voltage, or when the watchdog timeout period expires with no rising signal applied to the WD pin, until the RESETB pin output is released from the detection state. Five release delay time ($t_{DR}$) watchdog timeout period settings are available in 400ms, 200ms, 100ms, 50ms, and 3.13ms.

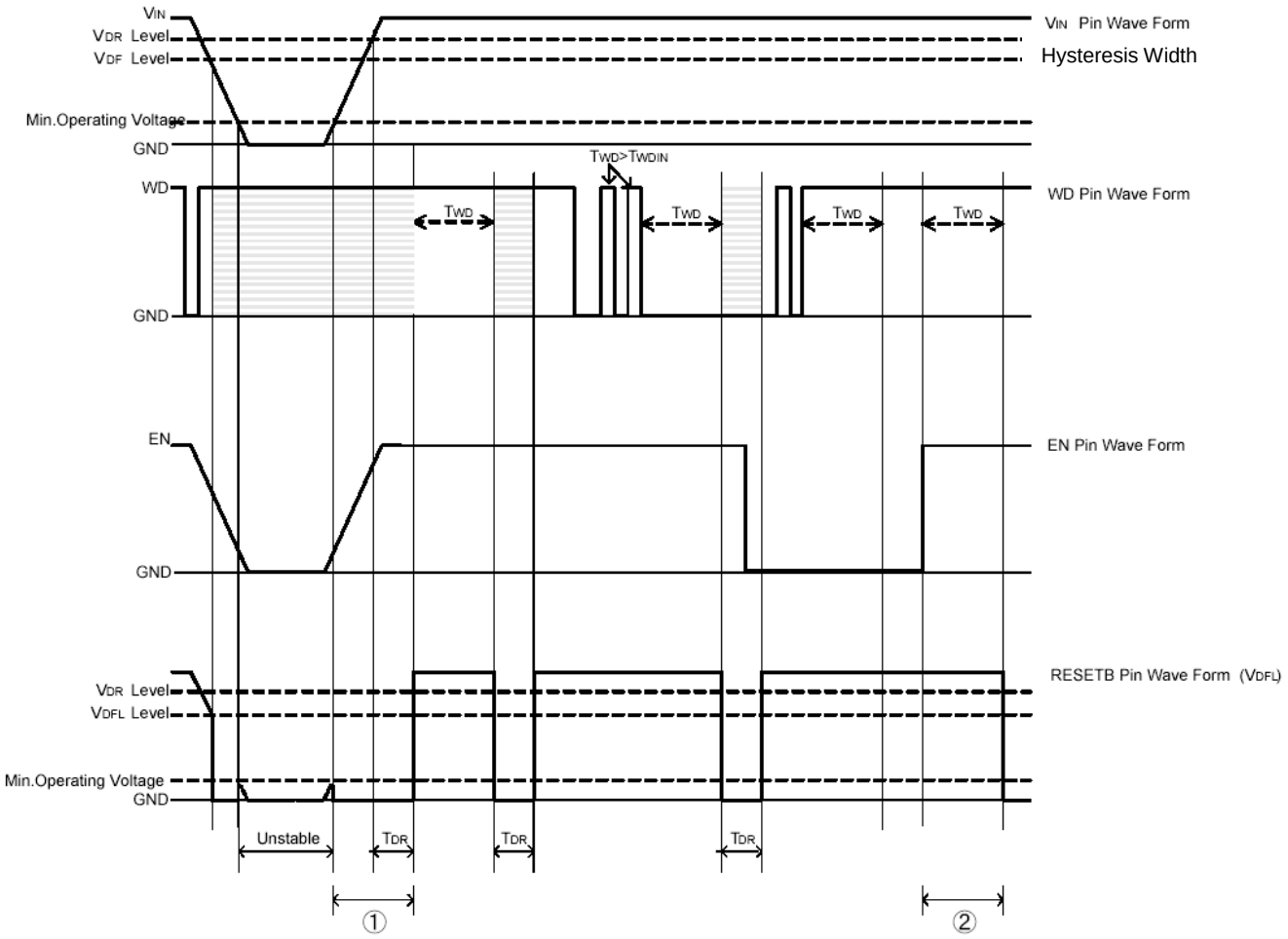
**<Detect Delay Time>**

Detect Delay Time ($t_{DF}$) is the time that elapses from when the $V_{IN}$ pin voltage falls to the detect voltage until the RESETB pin output goes into the detection state.

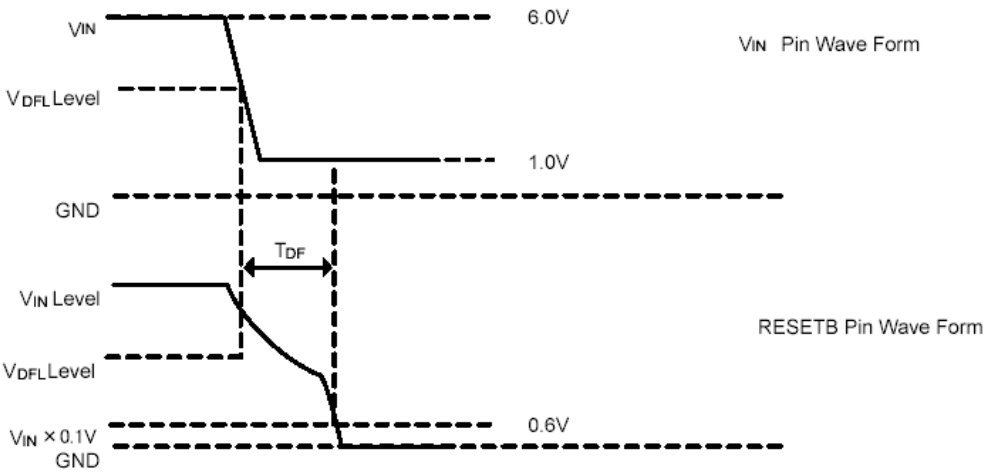
# ■TIMING CHARTS

1. XD6121/XD6122 Series (EN products)

●N-ch Open Drain Output (Rpull=100kΩ)



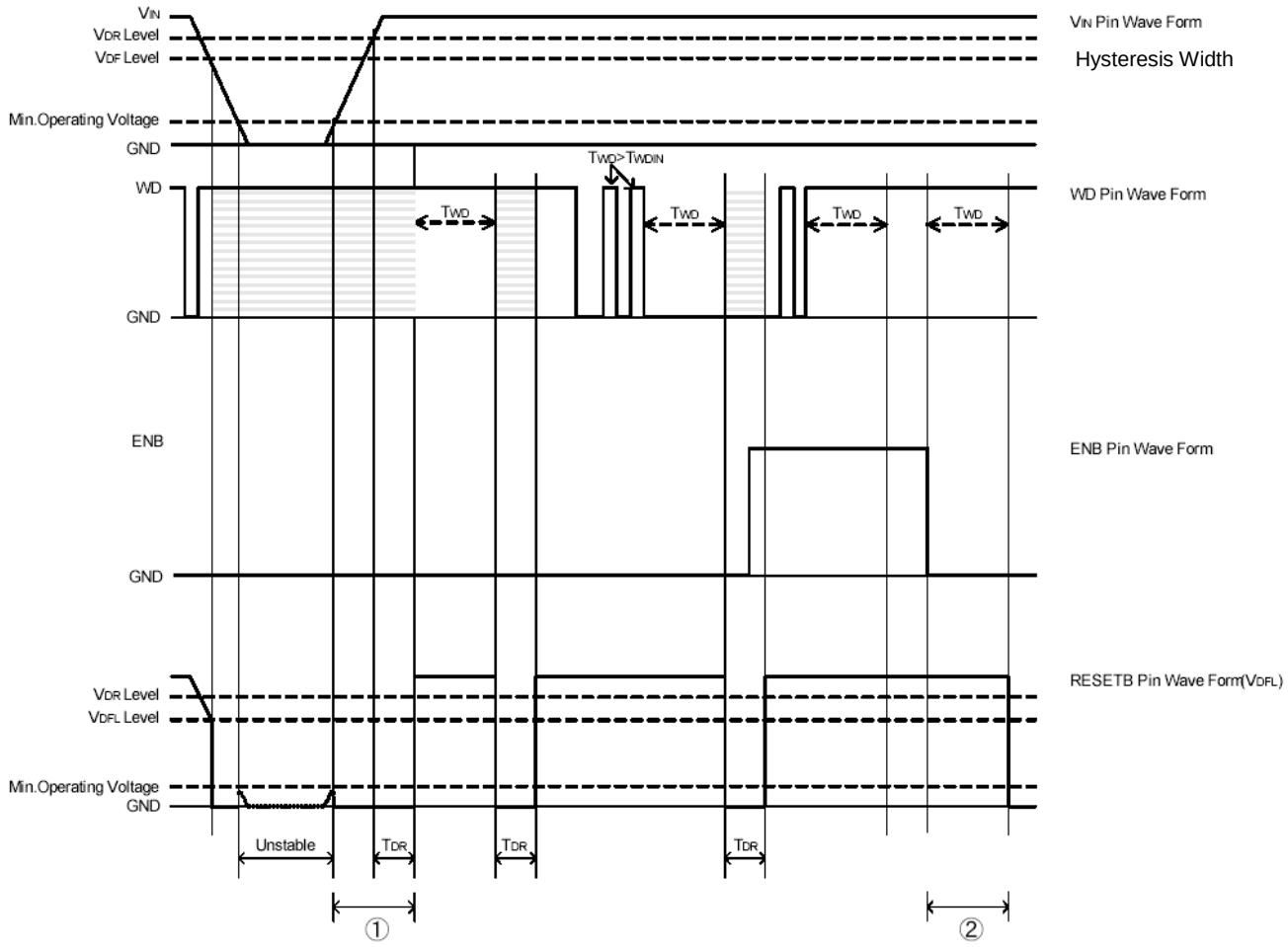

●$t_{DF}$ (N-ch Open Drain Output, Rpull=100kΩ)



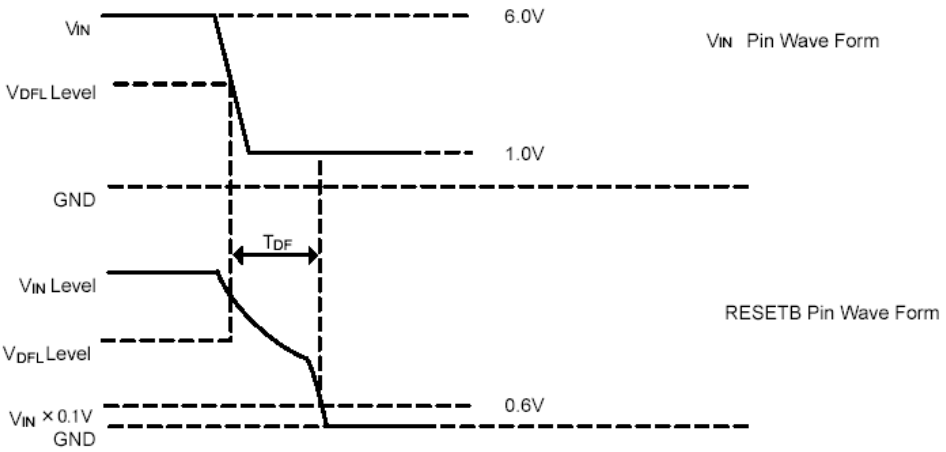
## ■TIMING CHARTS (Continued)

2. XD6123/XD6124 Series (ENB products)

●N-ch Open Drain Output (Rpull=100kΩ)




●tDF (N-ch Open Drain Output, Rpull=100kΩ)



# ■NOTES ON USE

1. Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

2. When a resistor is connected between the $V_{IN}$ pin and the input, the $V_{IN}$ voltage drops while the IC is operating and a malfunction may occur as a result of the IC's through current.

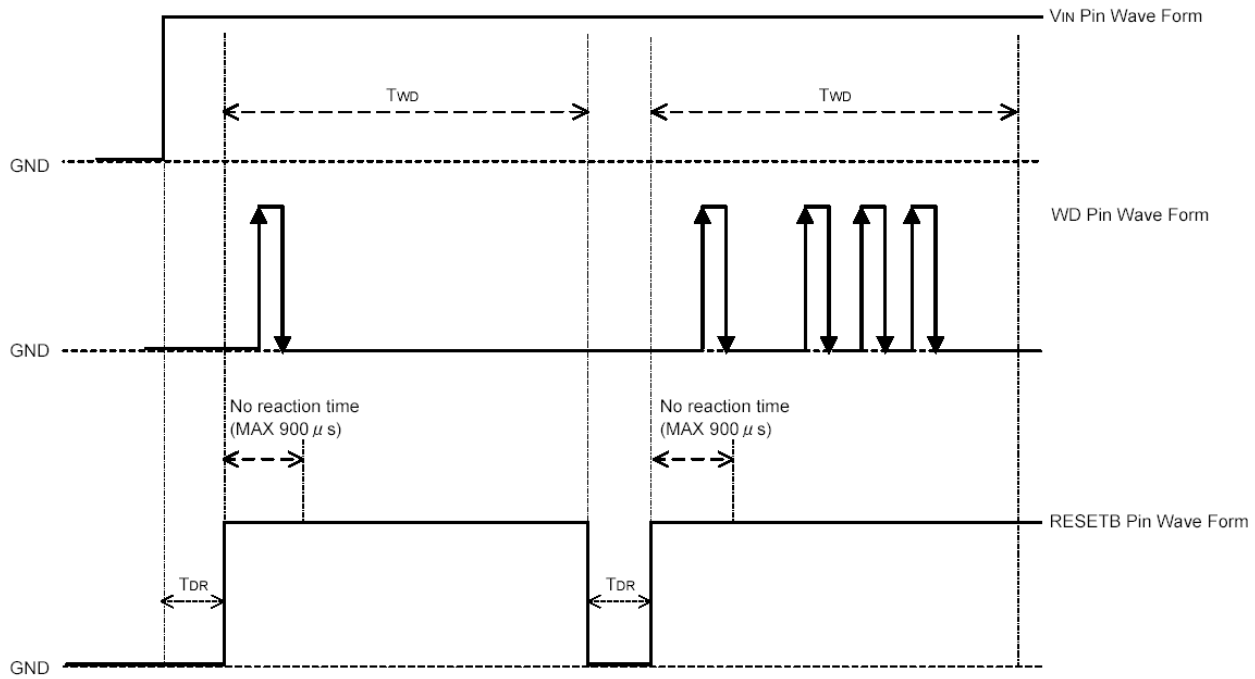
3. In order to stabilize the IC's operations, please ensure that the $V_{IN}$ pin's input frequency's rise and fall times are more than 1 μ s/V.

4. Noise at the power supply may cause a malfunction of the watchdog operation or the voltage detector. In such case, please strength $V_{IN}$ and GND lines. Also, please connect a capacitor such as 0.22 μF between the $V_{IN}$ pin and the GND pin and evaluate the device on the actual board carefully before use.

5. Protecting against a malfunction while the watchdog time out period, an ignoring time (no reaction time) occurs to the rise and fall times. Referring to the figure below, the ignoring time (no reaction time) lasts for 900 μs at maximum. (refer to the Figure1 below)

6. The EN pin of the XD6121 series is not internally pulled up. When using the watchdog function, please drive the $V_{EN}$ pin in high level. The EN pin of the XD6122 series is internally pulled up. The watchdog function can be used even the EN pin left open. The ENB pin of the XD6123 series is not internally pulled down. When using the watchdog function, please drive the $V_{ENB}$ pin in low level. The ENB pin of the XD6124 series is internally pulled down. The watchdog function can be used even the ENB pin left open.

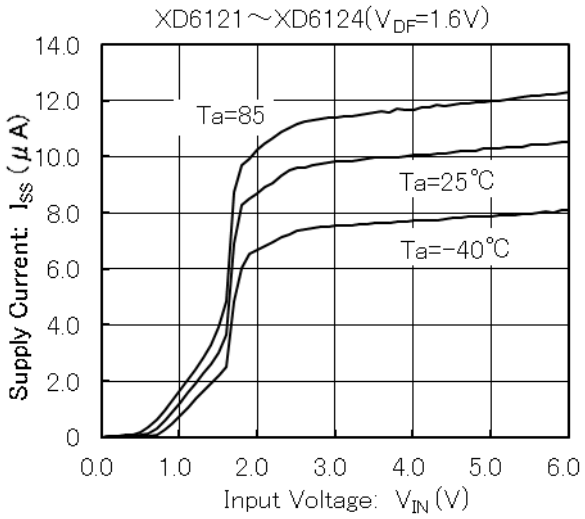
7. Torex places an importance on improving our products and its reliability.
However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.

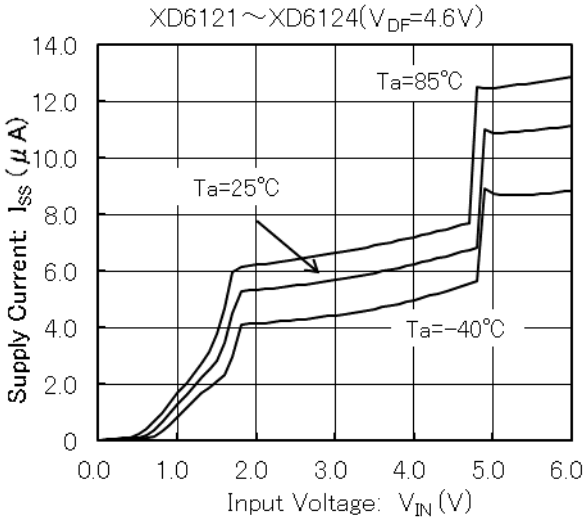



[Figure1]

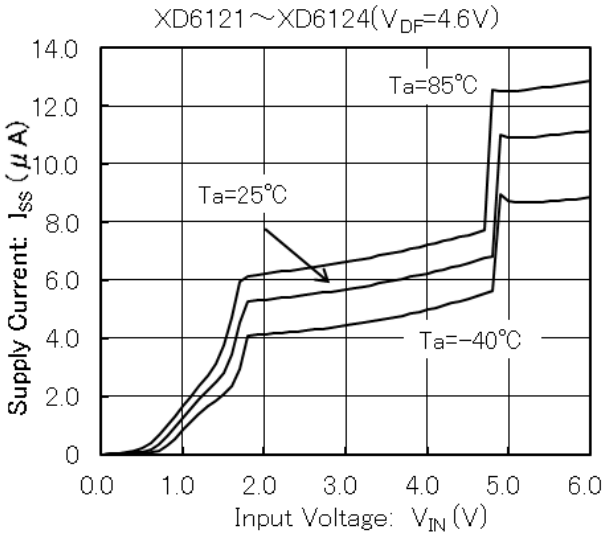
## ■TYPICAL PERFORMANCE CHARACTERISTICS

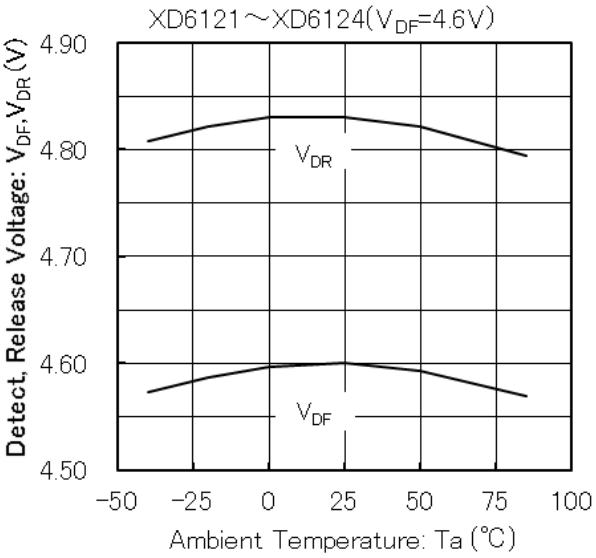
（1.） Supply Current vs. Input Voltage



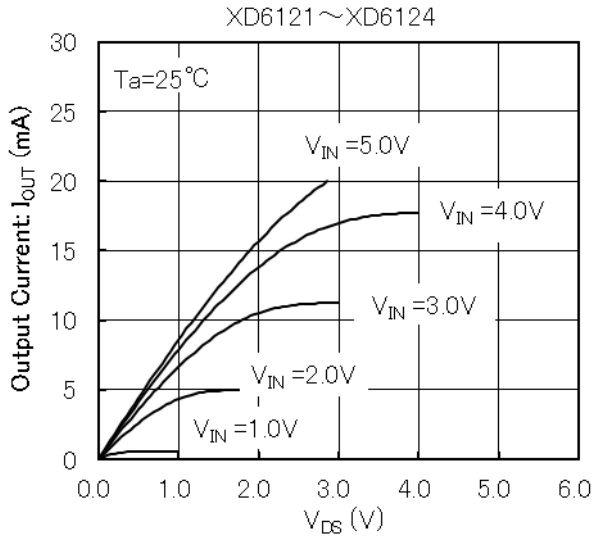




（2.） Ambient Temperature vs. Detect Release Voltage

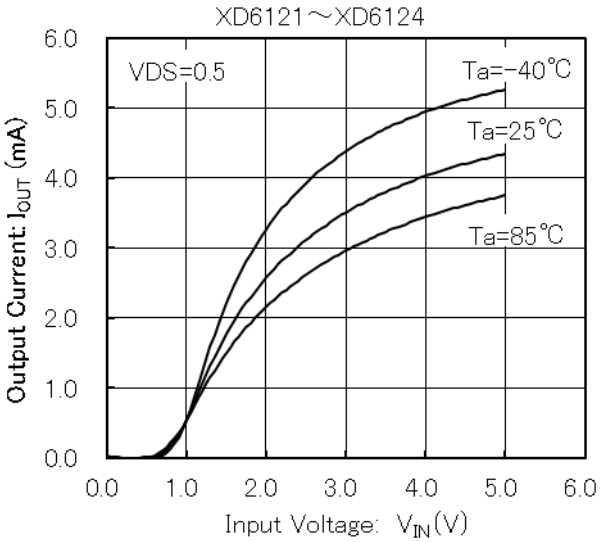



（3.） Output Current vs. VDS

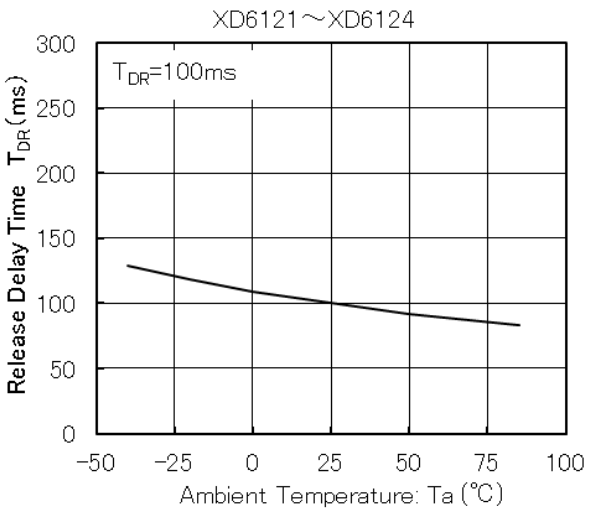


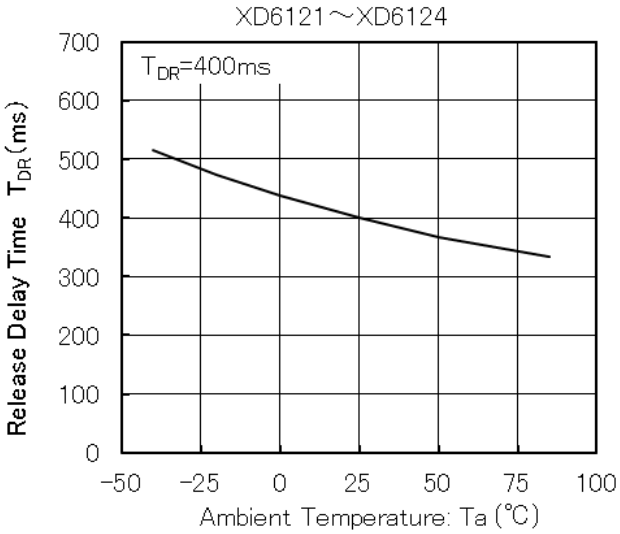

（4.） Output Current vs. Input Voltage



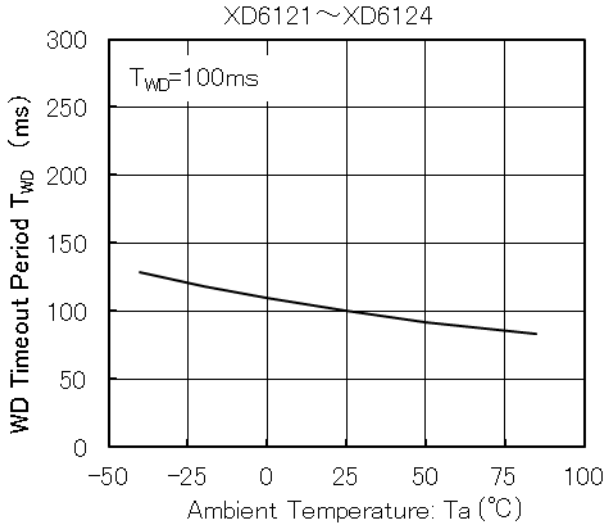
# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

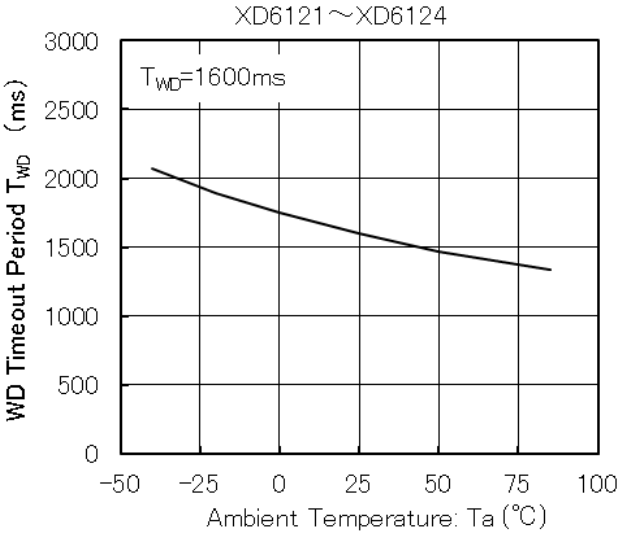
（5.） Release Delay Time vs. Ambient Temperature



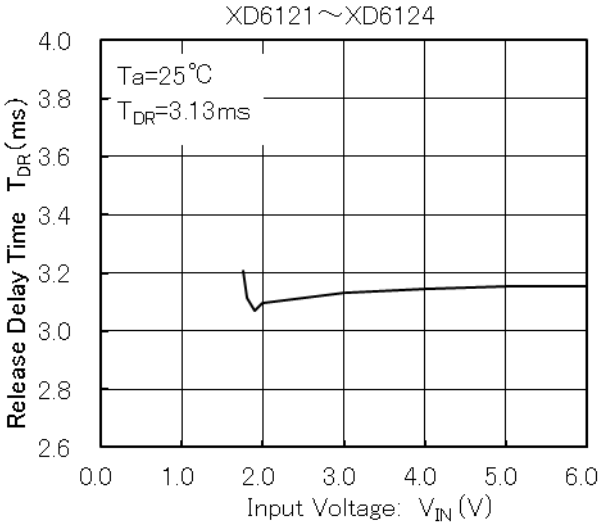




（6.） WD Timeout Period vs. Ambient Temperature

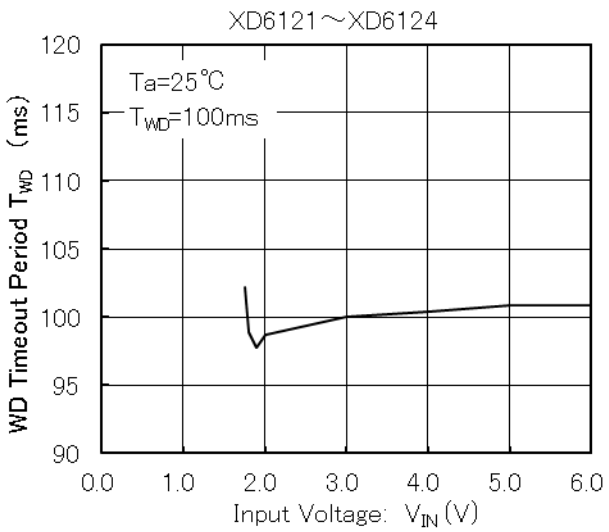



（7.） Release Delay Time vs. Input Voltage

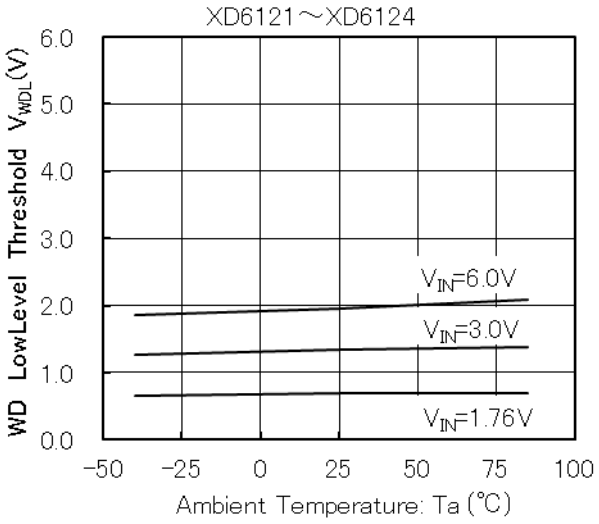



（8.） WD Timeout Period vs. Input Voltage

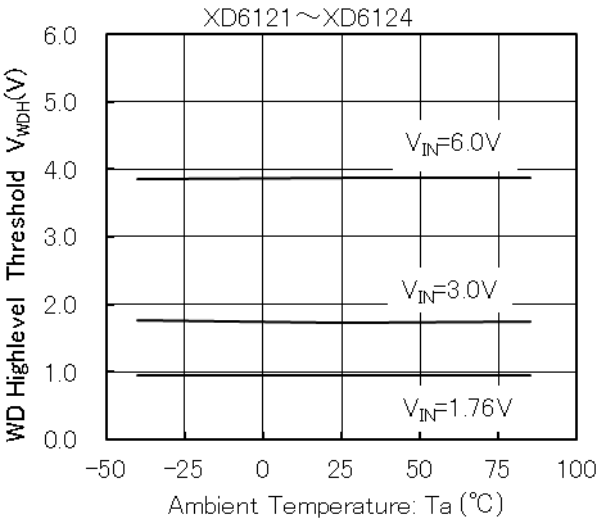


## ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

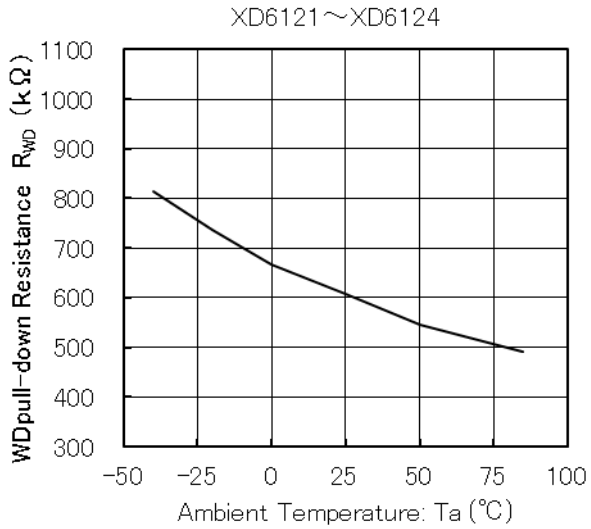
(9.) WD Low Level Voltage vs. Ambient Temperature



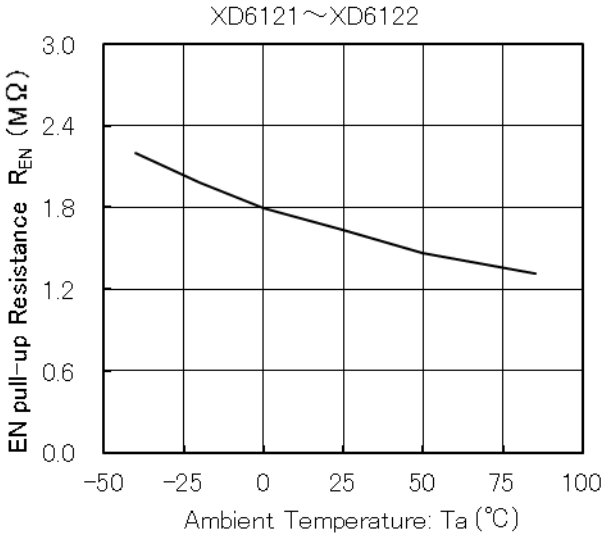

(10.) WD High Level Voltage vs. Ambient Temperature



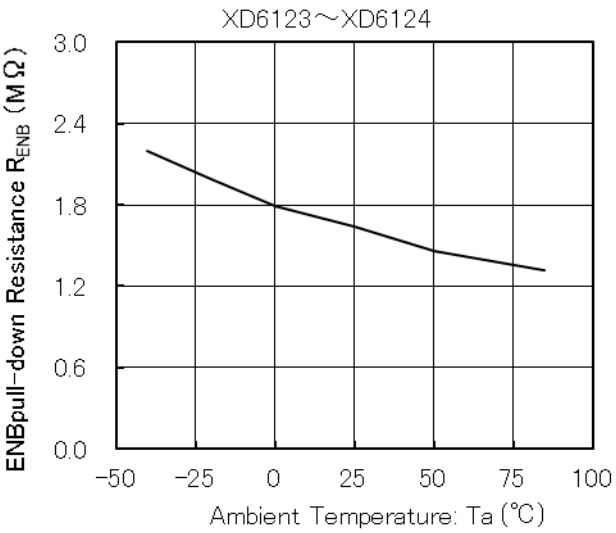

(11.) WD pull-down Resistance vs. Ambient Temperature




(12.) EN pull-up Resistance vs. Ambient Temperature

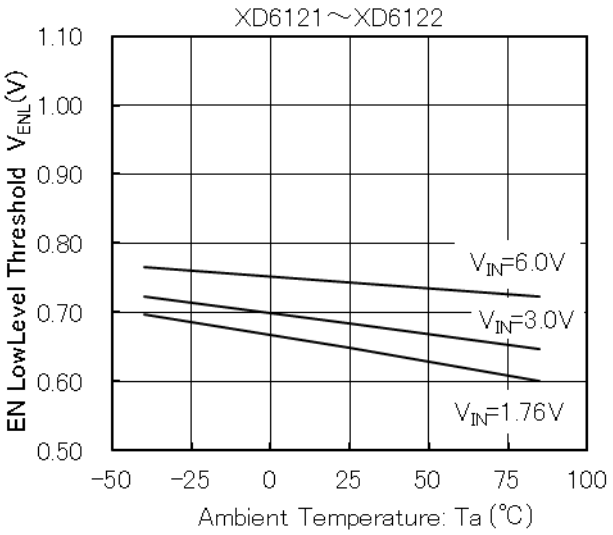



(13.) ENB pull-up Resistance vs. Ambient Temperature

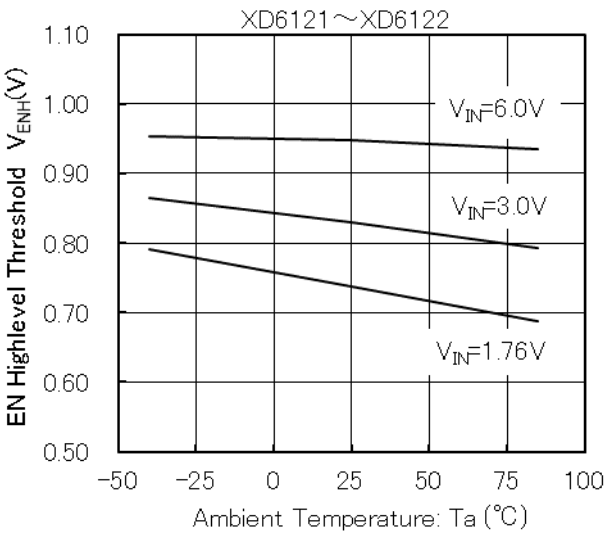


# ■TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

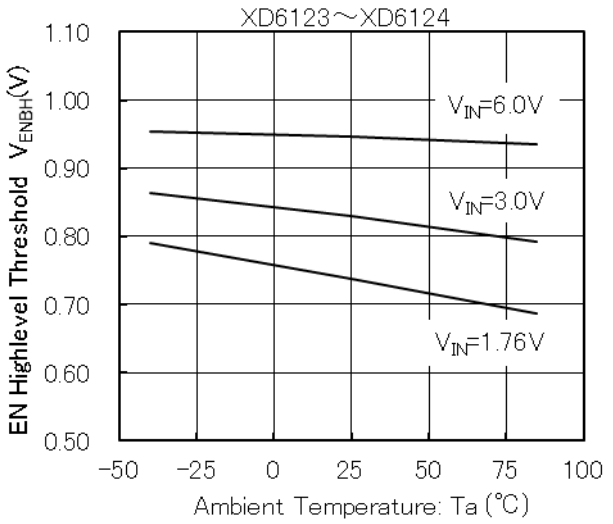
（14.）EN Low Level Voltage vs. Ambient Temperature



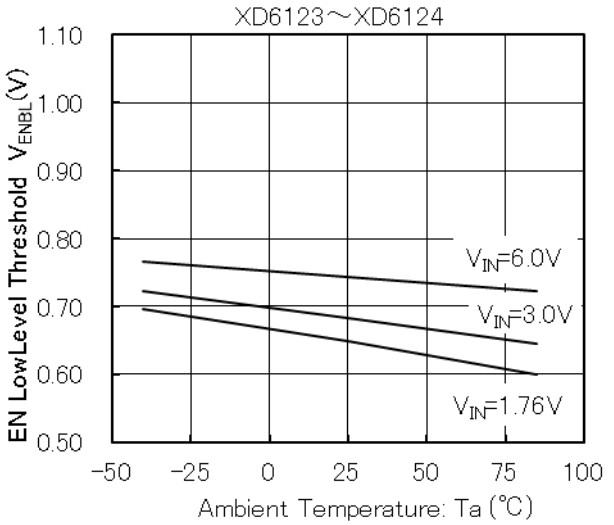

（15.）EN High Level Voltage vs. Ambient Temperature




（16.）ENB Low Level Voltage vs. Ambient Temperature




（17.）ENB High Level Voltage vs. Ambient Temperature



# ■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

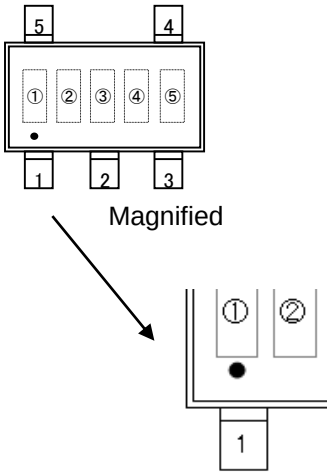
| PACKAGE | OUTLIN / LAND PATTERN | THERMAL CHARACTERISTICS | |
|---|---|---|---|
| SOT-25 | SOT-25 PKG | Standard Board | SOT-25 Power Dissipation |
| | | JESD51-7 Board | |

# ■MARKING RULE

① represents products series

| MARK | PRODUCT SERIES |
|---|---|
| B | XD6121/XD6122/XD6123/XD6124******-Q |

SOT-25(Under dot)




②③ represents internal sequential number.

01、…、09、10、…、99、A0、…、A9、B0、…、B9、…、Z9… repeated.

(G, I, J, O, Q, W excluded)

| MARK | PRODUCT SERIES |
|---|---|
| 01 | XD6121A246MR-Q |
| 02 | XD6122C629MR-Q |
| 03 | XD6123C330MR-Q |
| 04 | XD6124E616MR-Q |
| 05 | XD6121C622MR-Q |
| 06 | XD6122C645MR-Q |
| 07 | XD6121C229MR-Q |
| 08 | XD6122C229MR-Q |
| 09 | XD6122C630MR-Q |
| 10 | XD6121A430MR-Q |

④⑤ represents production lot number

01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order.(G, I, J, O, Q, W excluded)

* No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.
2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.
3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.
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   Do not use the product for in-vehicle use or other uses unless agreed by us in writing in advance.
5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.
6. Our products are not designed to be Radiation-resistant.
7. Please use the product listed in this datasheet within the specified ranges.
8. We assume no responsibility for damage or loss due to abnormal use.
9. 

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