

# XD6132 Series

ETR02043-002

Delay capacitor adjustable voltage detectors with sense pin isolation, surge voltage protection and HYS external adjustment

☆AEC-Q100 Grade1

## ■ GENERAL DESCRIPTION

The XD6132 series are ultra-small delay capacitor adjustable type voltage detectors that have high accuracy and sense pin isolation. High accuracy and a low supply current are achieved by means of a CMOS process, a highly accurate reference power supply, and laser trimming technology.

The sense pin is isolated from the power input pin to enable monitoring of the voltage of another power supply. Output can be maintained in the detection state even if the voltage of the power supply that is monitored drops to 0V. The sense pin is also suitable for detecting high voltages, and the detection and release voltage can be set as desired using external resistors. An internal surge voltage protection circuit and an internal delay circuit are also provided.

By connecting a capacitor to the Cd/MRB pin, any release delay time and detect delay time can be set and the pin can also be used as a manual reset pin.

The HYS external adjustment pin can be used to establish a sufficient hysteresis width.

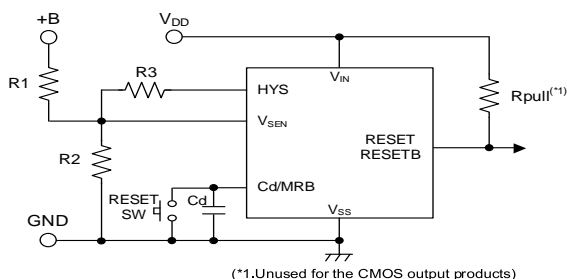
## ■ APPLICATIONS

- Car navigation systems
- Car audios
- Automotive Camera
- Other automotive equipment

## ■ FEATURES

Operating Ambient Temperature	: -40°C~+125°C
Operating voltage range	: 1.6V~6.0V
Detect voltage(Standard)	: 1.0V
Detect voltage range(Semi-custom)	: 0.8V~2.0V
Detect voltage accuracy (Ta=25°C)	: ±18mV(V <sub>DF</sub> <1.5V) : ±1.2%(1.5V≤V <sub>DF</sub> ≤2.0V)
Detect voltage accuracy (Ta=-40~125°C)	: ±36mV(V <sub>DF</sub> <1.5V) : ±2.7%(1.5V≤V <sub>DF</sub> ≤2.0V)
Temperature Characteristics	: ±50ppm/°C(TYP.)
Hysteresis width	: V <sub>DF</sub> ×0.1%(TYP.)
Adjustable Pin for Hysteresis Width	: Yes
Low supply current	: 1.28μA(TYP.) V <sub>IN</sub> =1.6V(At detection) : 1.65μA(TYP.) V <sub>IN</sub> =6.0V(At release)
Manual reset function	: Yes (For details, refer to FUNCTION CHART)
Output type	: CMOS or Nch open drain
Output logic	: H level or L level at detection
Delay capacitance pin	: Release delay / detection delay can be set in 4 time ratio options (For details, refer to Selection Guide).
Sense pin	: Includes a surge voltage protection function
Packages	: USP-6C,SOT-26
Environment friendly	: EU RoHS compliant, Pb free

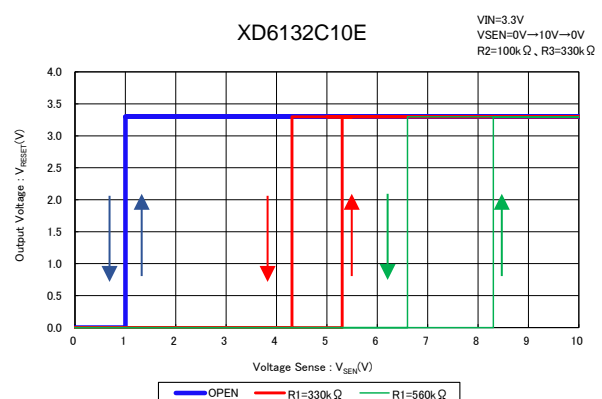
## ■ TYPICAL APPLICATION CIRCUIT



Battery (+B) voltage monitoring: Detects high voltage via R1/R2 resistance division.

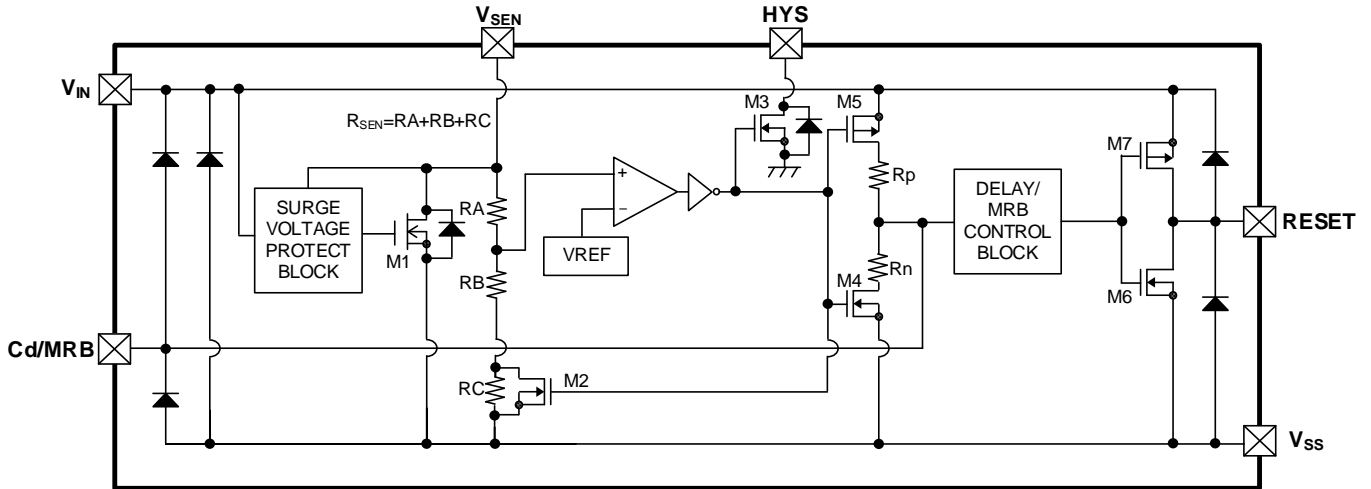
A hysteresis width can be added as desired by connecting R3 between the V<sub>SEN</sub> and HYS pins (For details, refer to OPERATIONAL DESCRIPTION).

## ■ TYPICAL PERFORMANCE CHARACTERISTICS



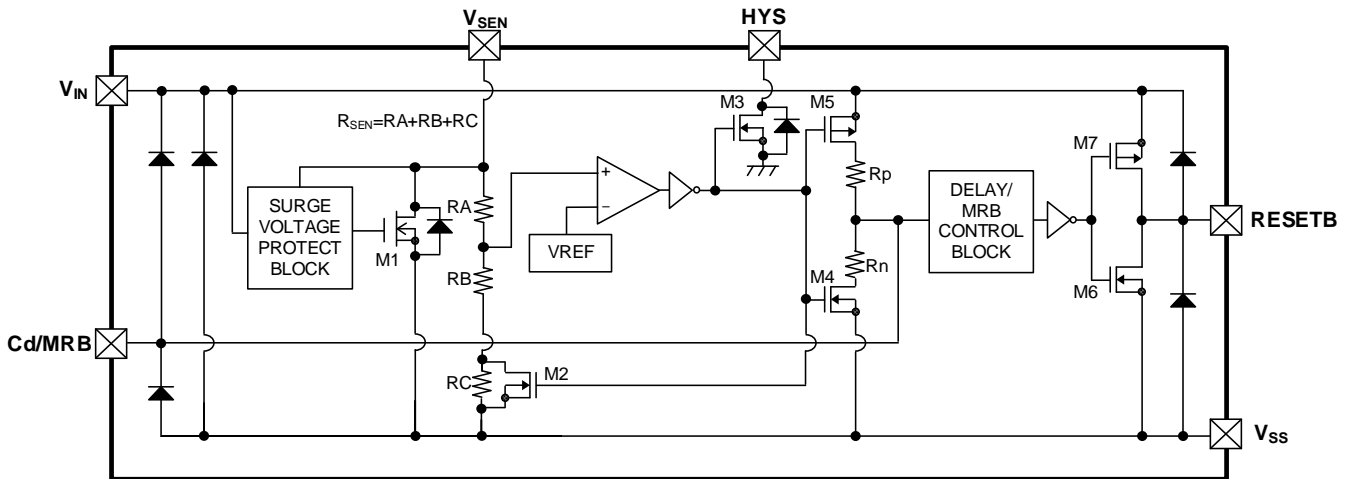
## ■ BLOCK DIAGRAMS

(1)XD6132C Series A/B/C/D type (RESET OUTPUT: CMOS/Active High)



\* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

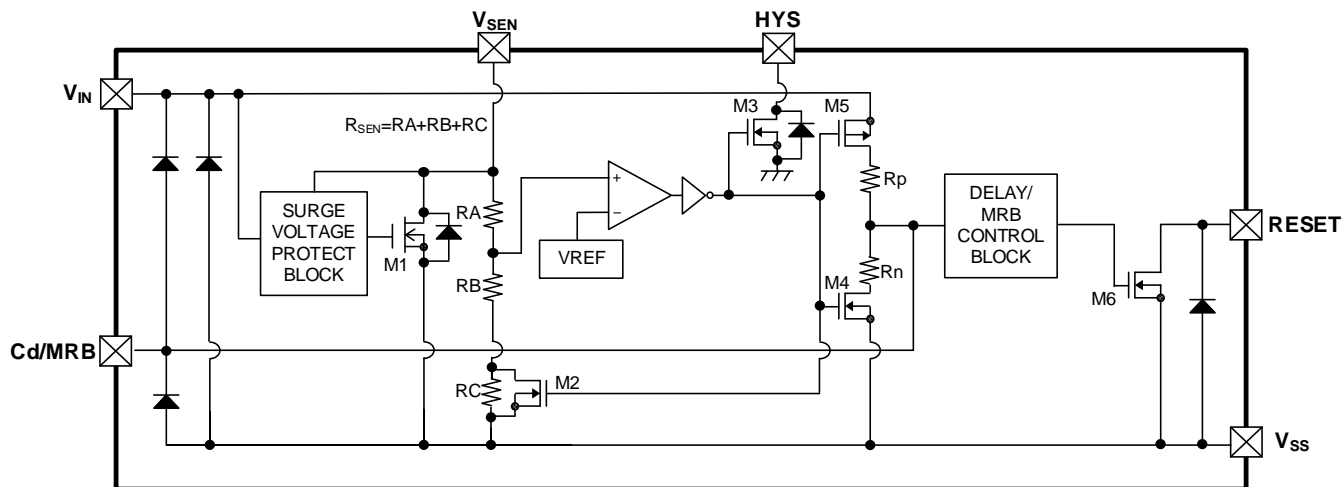
(2)XD6132C Series E/F/H/K type (RESETB OUTPUT: CMOS/Active Low)



\* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

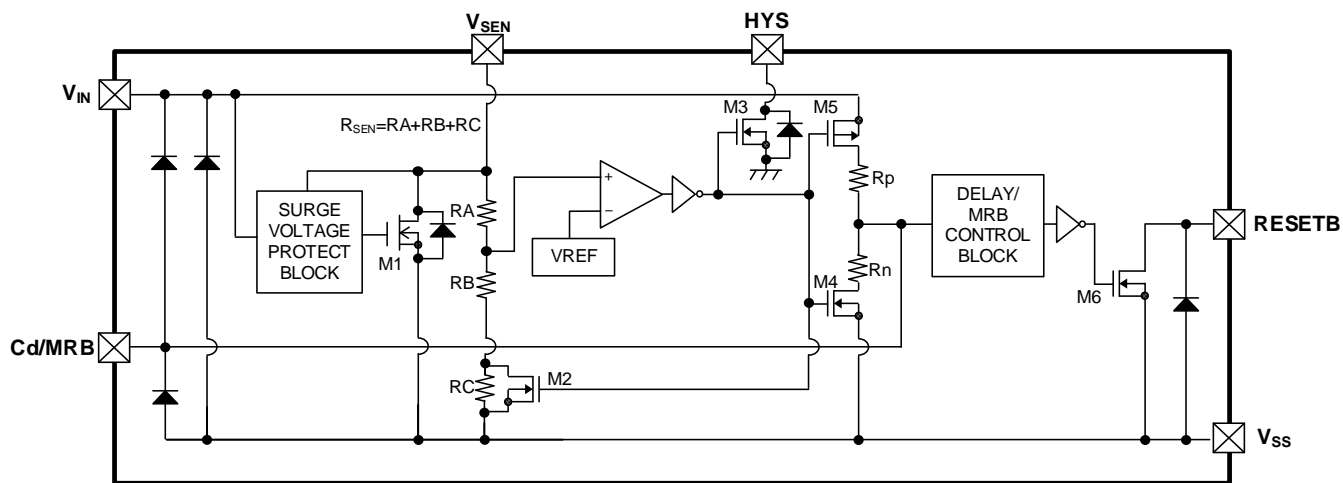
■ **BLOCK DIAGRAMS (Continued)**

(3)XD6132N Series A/B/C/D type (RESET OUTPUT: Nch open drain/Active High)



\* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

(4)XD6132N Series E/F/H/K type (RESETB OUTPUT: Nch open drain/Active Low)



\* Diodes inside the circuit are an ESD protection diode and a parasitic diode.

## ■ PRODUCT CLASSIFICATION

### ● Ordering Information

XD6132①②③④⑤⑥-⑦<sup>(\*)</sup>

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	Nch open drain output
②③	Detect Voltage	10 <sup>(2)</sup>	e.g. 1.0V → ②=1, ③=0
④	Type	A~K	Refer to Selection Guide
⑤⑥-⑦ <sup>(*)</sup>	Packages (Order Unit)	MR-Q	SOT-26 (3,000pcs/Reel)
		ER-Q	USP-6C (3,000pcs/Reel)

<sup>(1)</sup> The "-Q" suffix denotes "AEC-Q100" and "Halogen and Antimony free" as well as being fully EU RoHS compliant.

<sup>(2)</sup> For other output voltages, please contact your local Torex sales office or representative. The output voltage optional range is 0.8V to 2.0V.

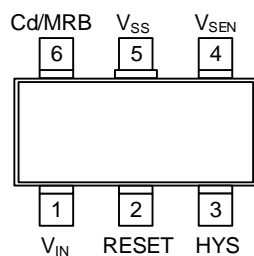
### ● Selection Guide

Part No.	Output Configuration	Detect Voltage	RESET/RESETB OUTPUT	DELAY(Rp:Rn)		HYSTERESIS	
XD6132C10A	CMOS output	1.0V	Active High <sup>(3)</sup>	1:0	144kΩ:0Ω	0.1% (TYP.)	
XD6132C10B		↑	↑	1:0.125	144kΩ:18kΩ	↑	
XD6132C10C		↑	↑	1:1	144kΩ:144kΩ	↑	
XD6132C10D		↑	↑	2:1	288kΩ:144kΩ	↑	
XD6132C10E		↑	Active Low <sup>(3)</sup>	1:0	144kΩ:0Ω	↑	
XD6132C10F		↑	↑	1:0.125	144kΩ:18kΩ	↑	
XD6132C10H		↑	↑	1:1	144kΩ:144kΩ	↑	
XD6132C10K		↑	↑	2:1	288kΩ:144kΩ	↑	
XD6132N10A		Nch open drain output	↑	Active High <sup>(3)</sup>	1:0	144kΩ:0Ω	↑
XD6132N10B			↑	↑	1:0.125	144kΩ:18kΩ	↑
XD6132N10C	↑		↑	1:1	144kΩ:144kΩ	↑	
XD6132N10D	↑		↑	2:1	288kΩ:144kΩ	↑	
XD6132N10E	↑		Active Low <sup>(3)</sup>	1:0	144kΩ:0Ω	↑	
XD6132N10F	↑		↑	1:0.125	144kΩ:18kΩ	↑	
XD6132N10H	↑		↑	1:1	144kΩ:144kΩ	↑	
XD6132N10K	↑		↑	2:1	288kΩ:144kΩ	↑	

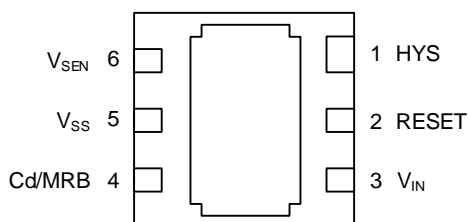
<sup>(3)</sup> "Active High" is H level when detection occurs, and "Active Low" is L level when detection occurs.

## ■ PIN CONFIGURATION

● A/B/C/D type

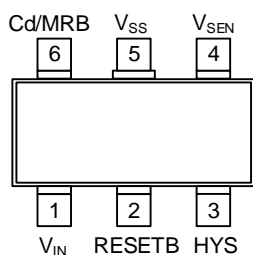


SOT-26  
(TOP VIEW)

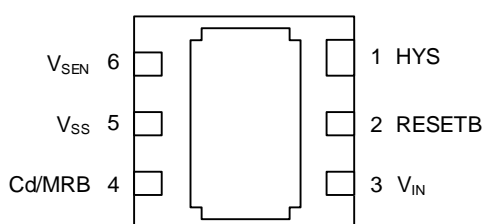


USP-6C  
(BOTTOM VIEW)

● E/F/H/K type



SOT-26  
(TOP VIEW)



USP-6C  
(BOTTOM VIEW)

\*The dissipation pad for the USP-6C package should be solder-plated in reference mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to  $V_{SS}$  (No.5) pin.

## ■ PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTIONS
SOT-26	USP-6C		
1	3	$V_{IN}$	Power Input
2	2	RESETB	Reset Output (Active Low) <sup>(*)</sup>
		RESET	Reset Output (Active High) <sup>(*)</sup>
3	1	HYS	Adjustable Pin for Hysteresis Width
4	6	$V_{SEN}$	Voltage Sense
5	5	$V_{SS}$	Ground
6	4	Cd/MRB	Adjustable Pin for Delay Time/ Manual Reset

<sup>(\*)</sup> Refer to the ④ in Ordering Information table.

## FUNCTION CHART

PIN NAME	SIGNAL	STATUS
Cd/MRB	L	Forced Reset
	H	For details, refer to " Function Chart "
	OPEN	Normal Operation

### Function Chart

$1.6V \leq V_{IN} \leq 6.0V$

$V_{SEN}$	$V_{Cd/MRB}$	Transition of $V_{RESETB}$ Condition	
		TYPE:A/B/C/D/L	TYPE:E/F/H/K/M
$V_{SEN} \geq V_{DF} + V_{HYS}$	$V_{Cd/MRB} \leq V_{MRL}$	Reset (High Level) <sup>(*)2</sup>	Reset (Low Level) <sup>(*)1</sup>
	$V_{Cd/MRB} \geq V_{MRH}$	Release (Low Level) <sup>(*)1</sup>	Release (High Level) <sup>(*)2</sup>
$V_{SEN} \leq V_{DF}$	$V_{Cd/MRB} \leq V_{MRL}$	Reset (High Level) <sup>(*)2</sup>	Reset (Low Level) <sup>(*)1</sup>
	$V_{Cd/MRB} \geq V_{MRH}$	Undefined <sup>(*)3</sup>	Undefined <sup>(*)3</sup>

<sup>(\*)1</sup> CMOS output:  $V_{IN} \times 0.1$  or less, N-ch open drain output, pull-up voltage  $\times 0.1$  or less.

<sup>(\*)2</sup> CMOS output:  $V_{IN} \times 0.9$  or higher, N-ch open drain output, pull-up voltage  $\times 0.9$  or higher.

<sup>(\*)3</sup> For details, refer to ■ OPERATIONAL DESCRIPTION < Manual reset function >.

Note: If used with  $V_{IN} < V_{SEN}$ , the surge protection circuit will activate. Use with  $V_{IN} \geq V_{SEN}$ .

## ABSOLUTE MAXIMUM RATINGS

$T_a = 25^\circ\text{C}$

PARAMETER		SYMBOL		RATINGS	UNITS	
Input Voltage		$V_{IN}$		-0.3~+7.0	V	
$V_{SEN}$ Pin Voltage		$V_{SEN}$		-0.3~+ $V_{IN}+0.3$ or +7.0 <sup>(*)1</sup>	V	
HYS Pin Voltage		$V_{HYS}$		-0.3~+7.0	V	
Cd/MRB Pin Voltage		$V_{Cd/MRB}$		-0.3~+ $V_{IN}+0.3$ or +7.0 <sup>(*)1</sup>	V	
Output Voltage	XD6132C <sup>(*)2</sup>	$V_{RESETB}$	$V_{RESET}$	-0.3~+ $V_{IN}+0.3$ or +7.0 <sup>(*)1</sup>	V	
	XD6132N <sup>(*)3</sup>			-0.3~+7.0	V	
Cd/MRB Pin Current		$I_{Cd/MRB}$		$\pm 5.0$	mA	
Output Current	XD6132C <sup>(*)2</sup>	$I_{RBOUT}$	$I_{ROUT}$	$\pm 50$	mA	
	XD6132N <sup>(*)3</sup>			+50	mA	
HYS Pin Current		$I_{HYS}$		+50	mA	
$V_{SEN}$ Pin Surge Current(+)		$I_{SENSURGE(+)}$		+2.5 <sup>(*)4</sup>	mA	
$V_{SEN}$ Pin Surge Current(-)		$I_{SENSURGE(-)}$		-2.5 <sup>(*)5</sup>	mA	
$V_{SEN}$ Pin Surge Voltage(+)		$V_{SENSURGE(+)}$		+7.0 <sup>(*)4</sup>	V	
$V_{SEN}$ Pin Surge Voltage(-)		$V_{SENSURGE(-)}$		-0.9 <sup>(*)5</sup>	V	
Power Dissipation	SOT-26	Pd		250	mW	
				600 (40mm x 40mm Standard Board) <sup>(*)6</sup>		
	USP-6C			100		mW
				1250 ( JESD51-7Board) <sup>(*)6</sup>		
Operating Ambient Temperature		$T_{opr}$		-40~+125	$^\circ\text{C}$	
Storage Temperature		$T_{stg}$		-55~+125	$^\circ\text{C}$	

\* All voltages are described based on the  $V_{SS}$ .

<sup>(\*)1</sup> The maximum value should be either  $V_{IN}+0.3$  or +7.0 in the lowest.

<sup>(\*)2</sup> CMOS Output

<sup>(\*)3</sup> N-ch Open Drain Output

<sup>(\*)4</sup> Transient  $\leq 200\text{ms}$ .

<sup>(\*)5</sup> Transient  $\leq 20\text{ms}$ .

<sup>(\*)6</sup> The power dissipation figure shown is PCB mounted and is for reference only.

Please see the power dissipation page for the mounting condition.

## ■ ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	Ta=25°C			-40°C ≤ Ta ≤ 125°C <sup>(*)</sup>			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Operating Voltage	V <sub>IN</sub>		1.6		6.0	1.6		6.0	V	①
V <sub>SEN</sub> Input Voltage	V <sub>SEN</sub>		0		6.0	0		6.0	V	
Detect Voltage	V <sub>DF</sub>		0.982	1.000	1.018	0.964	1.000	1.036	V	
Hysteresis Width	V <sub>HYS</sub>		-	V <sub>DF</sub> ×0.001	V <sub>DF</sub> ×0.007	-	V <sub>DF</sub> ×0.001	V <sub>DF</sub> ×0.01	V	
Supply Current 1	I <sub>ss1</sub>	V <sub>SEN</sub> =V <sub>DF</sub> ×0.9V, V <sub>IN</sub> =1.6V	-	1.28	2.65	-	1.28	3.92	μA	②
		V <sub>SEN</sub> =V <sub>DF</sub> ×0.9V, V <sub>IN</sub> =6.0V	-	1.36	2.80	-	1.36	4.22		
Supply Current 2	I <sub>ss2</sub>	V <sub>SEN</sub> =V <sub>DF</sub> ×1.1V, V <sub>IN</sub> =1.6V	-	1.32	2.75	-	1.32	4.26		
		V <sub>SEN</sub> =V <sub>DF</sub> ×1.1V, V <sub>IN</sub> =6.0V	-	1.65	3.25	-	1.65	4.97		
SENSE Resistance	R <sub>SEN</sub>	V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =6.0V	10.0	26.1	-	7.6	26.1	-	MΩ	③
Release Delay Resistance (TYPE:A/B/C/E/F/H)	R <sub>p</sub>	V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =6.0V, V <sub>Cd/MRB</sub> =0V	130	144	158	122	144	166	kΩ	④
Release Delay Resistance (TYPE:D/K)		V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =6.0V, V <sub>Cd/MRB</sub> =0V	259	288	317	245	288	331		
Detect Delay Resistance (TYPE:C/D/H/K)	R <sub>n</sub>	V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =0V, V <sub>Cd/MRB</sub> =6.0V	130	144	158	122	144	166		
Detect Delay Resistance (TYPE:B/F)		V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =0V, V <sub>Cd/MRB</sub> =6.0V	16.8	18	19.1	16.2	18	19.8		
Release Delay Time <sup>(*)</sup>	t <sub>DRO</sub>	V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =V <sub>DF</sub> ×0.9V→V <sub>DF</sub> ×1.1V	-	20	102	-	20	136	μs	⑤
Detect Delay Time <sup>(*)</sup>	t <sub>DF0</sub>	V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =V <sub>DF</sub> ×1.1V→V <sub>DF</sub> ×0.9V	-	20	82	-	20	116		

Unless otherwise specified in measurement conditions, Cd/MRB pin and HYS pin are open.

This specification is 1.0V product. For other nominal output voltages of Electrical characteristics, please contact your local Torex sales office or representative.

<sup>(\*)</sup> RESETB product: Time from when the V<sub>SEN</sub> pin voltage reaches the release voltage until the reset output pin reaches 5.4V (V<sub>IN</sub>×90%).

RESET product: Time from when the V<sub>SEN</sub> pin voltage reaches the release voltage until the reset output pin reaches 0.6V (V<sub>IN</sub>×10%)

Release voltage (V<sub>DR</sub>)=Detect voltage (V<sub>DF</sub>)+Hysteresis width (V<sub>HYS</sub>).

<sup>(\*)</sup> RESETB product: Time from when the V<sub>SEN</sub> pin voltage reaches the detect voltage until the reset output pin reaches 0.6V (V<sub>IN</sub>×10%).

RESET product: Time from when the V<sub>SEN</sub> pin voltage reaches the detect voltage until the reset output pin reaches 5.4V (V<sub>IN</sub>×90%).

<sup>(\*)</sup> The ambient temperature range (-40°C ≤ Ta ≤ 125°C) is a design Value.

## ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	Ta=25°C			-40°C ≤ Ta ≤ 125°C <sup>(*)</sup>			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Hysteresis Output Current	I <sub>HYSOUT</sub>	V <sub>IN</sub> =1.6V, V <sub>SEN</sub> =0V, V <sub>HYS</sub> =0.3V	1.9	3.4	-	0.7	3.4	-	mA	⑥
Hysteresis Output Leakage Current	I <sub>HYSLEAK</sub>	V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =6.0V, V <sub>HYS</sub> =6.0V	-	0.01	0.1	-	0.01	1.0	μA	
RESETB Output Current	I <sub>RBOUTN</sub>	V <sub>SEN</sub> =V <sub>DF</sub> ×0.9V, Nch. V <sub>RESETB</sub> =0.3V							mA	⑦
		V <sub>IN</sub> =1.6V <sup>(*)</sup>	1.9	3.4	-	0.7	3.4	-		
		V <sub>IN</sub> =2.0V	4.2	6.0	-	2.0	6.0	-		
		V <sub>IN</sub> =3.0V	8.6	10.5	-	4.3	10.5	-		
		V <sub>IN</sub> =4.0V	12.7	14.1	-	6.2	14.1	-		
		V <sub>IN</sub> =5.0V	15.6	17.0	-	7.3	17.0	-		
	I <sub>RBOUTP</sub>	V <sub>SEN</sub> =V <sub>DF</sub> ×1.1V, Pch. V <sub>RESETB</sub> =V <sub>IN</sub> - 0.3V								
		V <sub>IN</sub> =1.6V <sup>(*)</sup>	-	-1.2	-0.7	-	-1.2	-0.48		
		V <sub>IN</sub> =3.0V	-	-3.0	-2.5	-	-3.0	-1.1		
		V <sub>IN</sub> =6.0V	-	-4.9	-4.4	-	-4.9	-2.5		
RESET Output Current	I <sub>ROUTN</sub>	V <sub>SEN</sub> =V <sub>DF</sub> ×1.1V, Nch. V <sub>RESET</sub> =0.3V							mA	⑦
		V <sub>IN</sub> =1.6V <sup>(*)</sup>	1.9	3.4	-	0.7	3.4	-		
		V <sub>IN</sub> =2.0V <sup>(*)</sup>	4.2	6.0	-	2.0	6.0	-		
		V <sub>IN</sub> =3.0V	8.6	10.5	-	4.3	10.5	-		
		V <sub>IN</sub> =4.0V	12.7	14.1	-	6.2	14.1	-		
		V <sub>IN</sub> =5.0V	15.6	17.0	-	7.3	17.0	-		
	I <sub>ROUTP</sub>	V <sub>SEN</sub> =V <sub>DF</sub> ×0.9V, Pch. V <sub>RESET</sub> =V <sub>IN</sub> -0.3V								
		V <sub>IN</sub> =1.6V <sup>(*)</sup>	-	-1.2	-0.7	-	-1.2	-0.48		
		V <sub>IN</sub> =3.0V	-	-3.0	-2.5	-	-3.0	-1.1		
		V <sub>IN</sub> =6.0V	-	-4.9	-4.4	-	-4.9	-2.5		
RESETB Output Leakage Current	I <sub>LEAKN</sub> <sup>(*)</sup>	V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =6.0V, Nch. V <sub>RESETB</sub> =6.0V	-	0.01	0.1	-	0.01	1.0	μA	⑦
	I <sub>LEAKP</sub>	V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =0V, Pch. V <sub>RESETB</sub> =0V	-	-0.01	-	-	-0.01	-		
RESET Output Leakage Current	I <sub>LEAKN</sub> <sup>(*)</sup>	V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =0V, Nch. V <sub>RESET</sub> =6.0V	-	0.01	0.1	-	0.01	1.0		
	I <sub>LEAKP</sub>	V <sub>IN</sub> =6.0V, V <sub>SEN</sub> =6.0V, Pch. V <sub>RESET</sub> =0V	-	-0.01	-	-	-0.01	-		

Unless otherwise specified in measurement conditions, Cd/MRB pin and HYS pin are open.

This specification is 1.0V product. For other nominal output voltages of Electrical characteristics, please contact your local Torex sales office or representative.

<sup>(\*)</sup> Max. value is for XD6132N (Nch open drain).

<sup>(\*)</sup> The ambient temperature range (-40°C ≤ Ta ≤ 125°C) is a design Value.



## ■ ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	Ta=25°C			-40°C ≤ Ta ≤ 125°C <sup>(*)8</sup>			UNITS	CIRCUIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Cd Pin Sink Current (TYPE:A/E)	I <sub>Cd</sub>	V <sub>IN</sub> =1.6V, V <sub>Cd/MRB</sub> =0.5V, V <sub>SEN</sub> =0V	0.92	1.2		0.66	1.2		mA	⑧
Cd Pin Threshold Voltage(Release)	V <sub>TCd1</sub>	V <sub>IN</sub> :Refer to V-1 <sup>(*)13</sup> , V <sub>SEN</sub> =0V→V <sub>DF</sub> ×1.1V	V <sub>IN</sub> ×0.46	V <sub>IN</sub> ×0.5	V <sub>IN</sub> ×0.54	V <sub>IN</sub> ×0.46	V <sub>IN</sub> ×0.5	V <sub>IN</sub> ×0.54	V	⑨
Cd Pin Threshold Voltage(Detect)	V <sub>TCd2</sub>	V <sub>IN</sub> :Refer to V-1 <sup>(*)13</sup> , V <sub>SEN</sub> =V <sub>DF</sub> ×1.1V→0V								
MRB High Level Voltage	V <sub>MRH</sub>	V <sub>IN</sub> :1.6V~6.0V, V <sub>SEN</sub> =V <sub>DF</sub> ×1.1V, V <sub>IN</sub> >V <sub>SEN</sub>	V <sub>IN</sub> ×0.55		V <sub>IN</sub>	V <sub>IN</sub> ×0.55		V <sub>IN</sub>	V	⑩
MRB Low Level Voltage	V <sub>MRL</sub>	V <sub>IN</sub> :1.6V~6.0V, V <sub>SEN</sub> =V <sub>DF</sub> ×1.1V, V <sub>IN</sub> >V <sub>SEN</sub>	0		V <sub>IN</sub> ×0.18	0		V <sub>IN</sub> ×0.18	V	
MRB Minimum Pulse Width	t <sub>MRIN</sub> <sup>(*)6</sup>	V <sub>IN</sub> =1.6V, V <sub>SEN</sub> =V <sub>DF</sub> ×1.1V, Apply pulse from V <sub>DF</sub> ×1.1V to 0V to the MRB pin.	5.0	-	-	5.0	-	-	μs	⑪
	t <sub>MRIN</sub> <sup>(*)7</sup>		32.0	-	-	32.0	-	-		

Unless otherwise specified in measurement conditions, Cd/MRB pin and HYS pin are open.

This specification is 1.0V product. For other nominal output voltages of Electrical characteristics, please contact your local Torex sales office or representative.

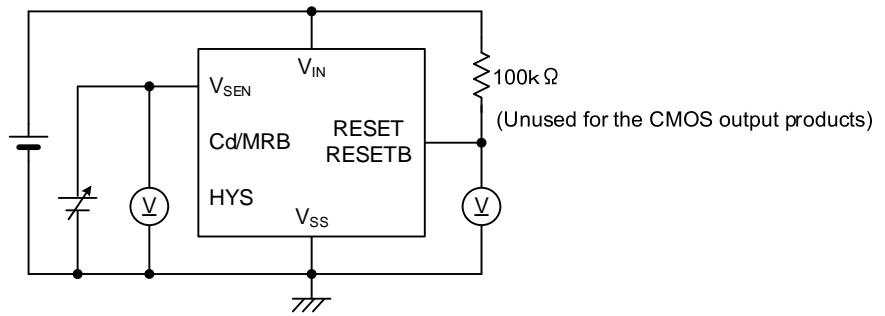
<sup>(\*)6</sup> Specification is guaranteed for types A/B/C/D/E/F/H/K of the CMOS output product and types E/F/H/K of the Nch open drain product.

<sup>(\*)7</sup> Specification is guaranteed for types A/B/C/D/L of the Nch open drain output product.

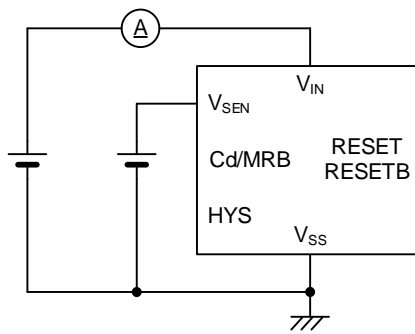
<sup>(\*)8</sup> The ambient temperature range (-40°C ≤ Ta ≤ 125°C) is a design Value.

## TEST CIRCUITS

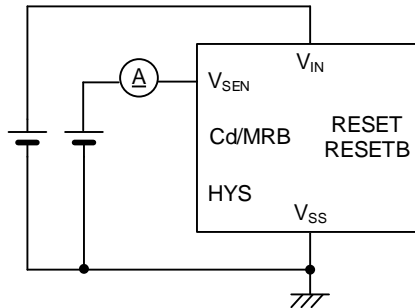
CIRCUIT①



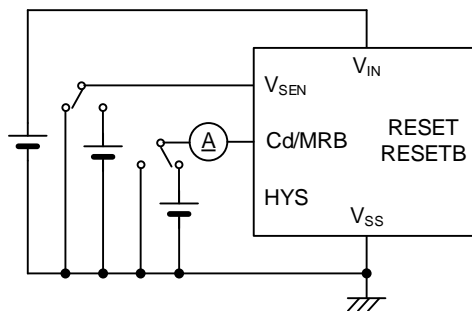
CIRCUIT②



CIRCUIT③



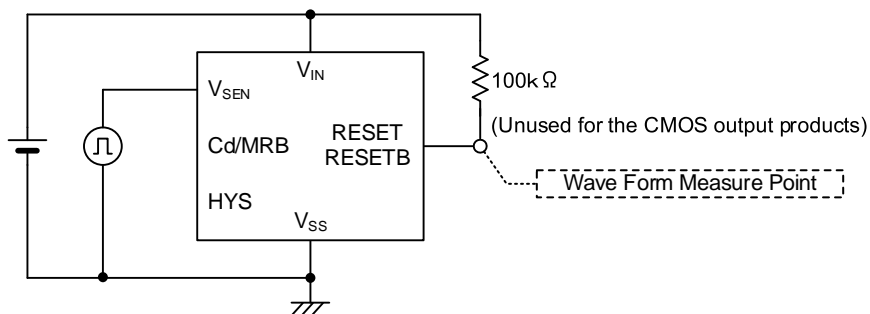
CIRCUIT④



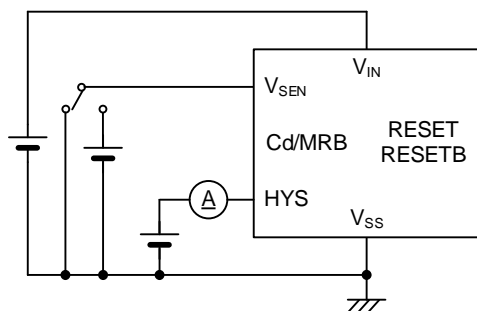
\*"RESET" is A/B/C/D/L type, and "RESETB" is E/F/H/K/M type.

■ TEST CIRCUITS (Continued)

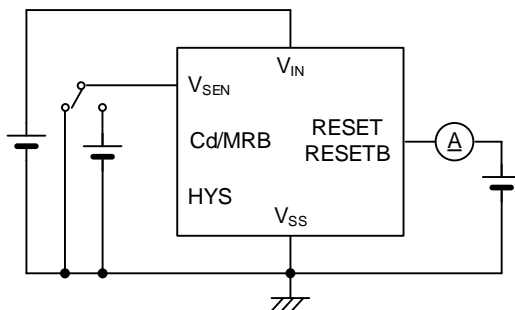
CIRCUIT⑤



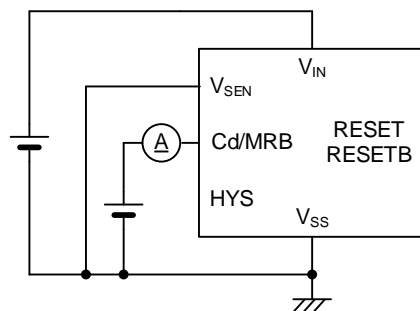
CIRCUIT⑥



CIRCUIT⑦



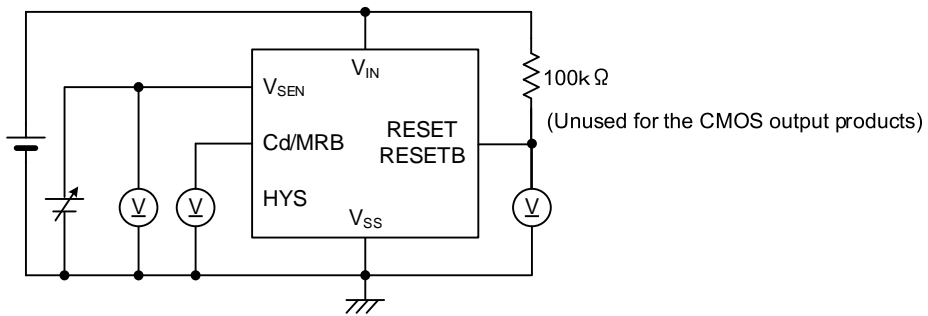
CIRCUIT⑧



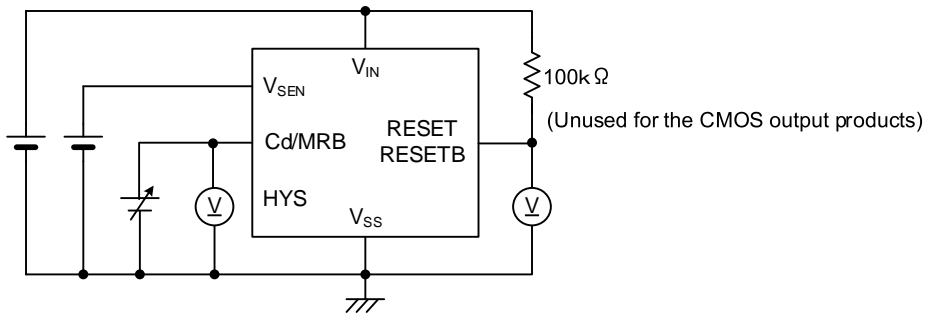
\*"RESET" is A/B/C/D/L type, and "RESETB" is E/F/H/K/M type.

## TEST CIRCUITS (Continued)

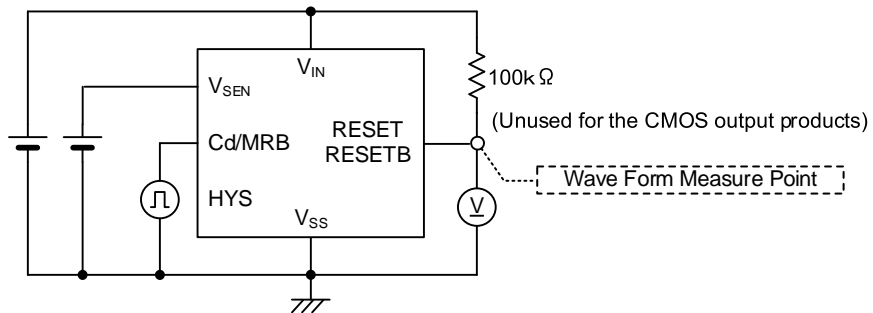
CIRCUIT⑨



CIRCUIT⑩



CIRCUIT⑪

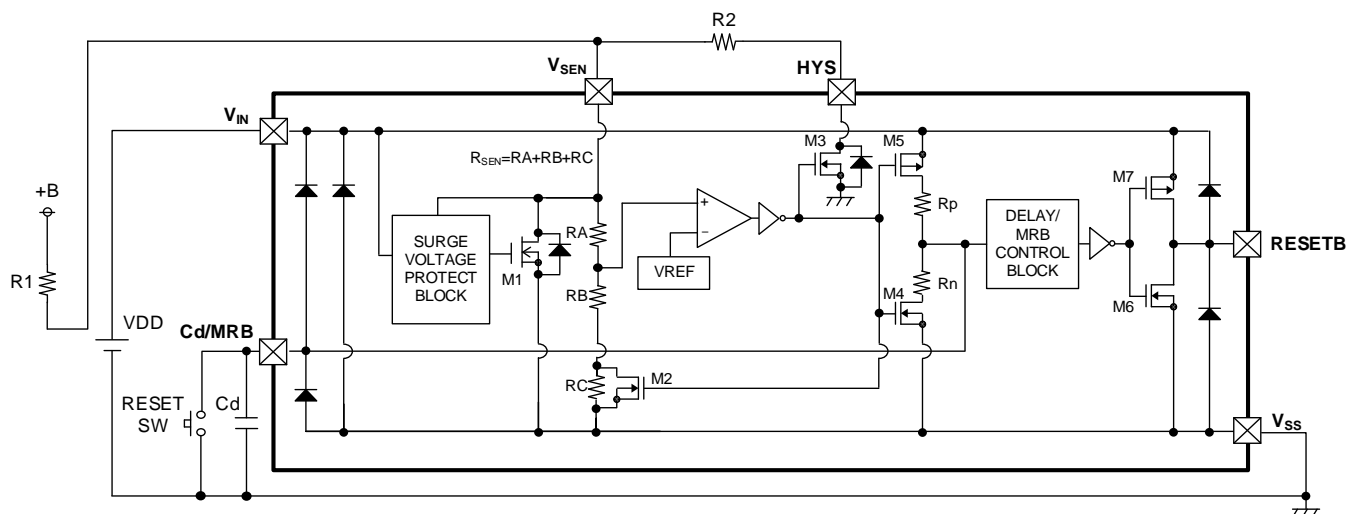


\*"RESET" is A/B/C/D/L type, and "RESETB" is E/F/H/K/M type.

## OPERATIONAL DESCRIPTION

### <Basic Operation>

Fig. 1 shows a typical block diagram. Fig. 2 shows the timing chart of Fig. 1.



\* The XD6132N series (N-ch open drain output) requires a resistor to pull up the output.

Fig. 1: Typical block diagram (Active Low product)

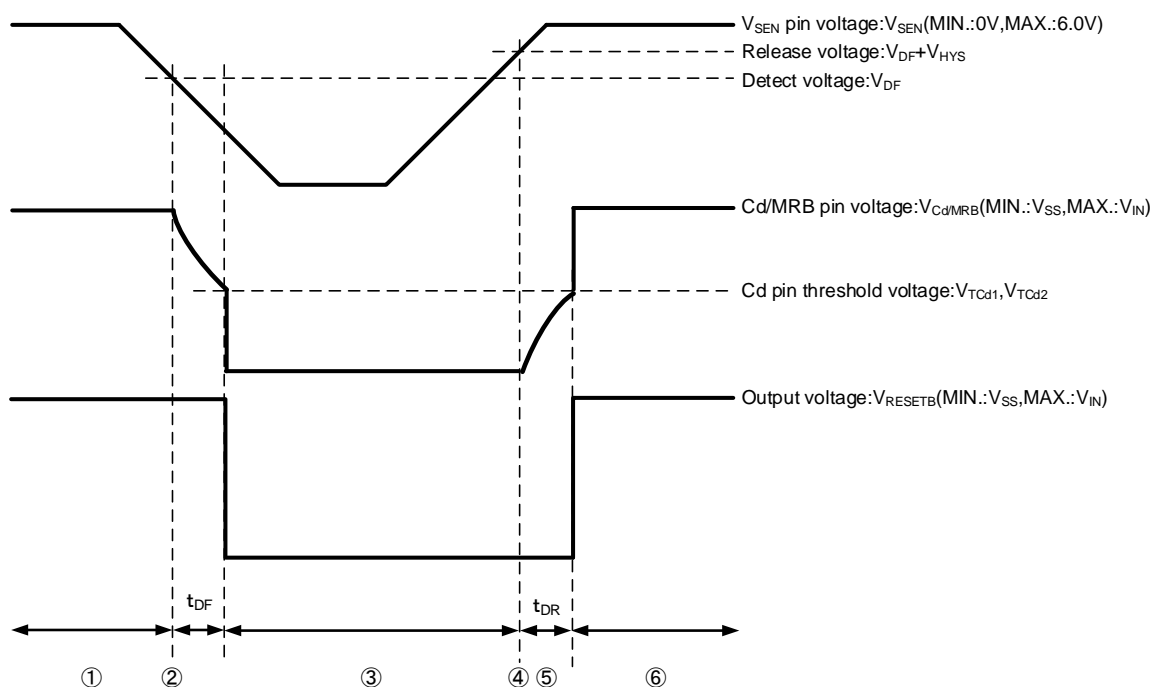


Fig. 2: Timing chart of Fig. 1 ( $V_{IN}=6.0V$ , Active Low product)

① In the initial state, a voltage that is sufficiently high (MAX.:6.0V) with respect to the release voltage is applied to the  $V_{SEN}$  pin, and the delay capacitance  $C_d$  is charged up to the power input pin voltage.

The  $V_{SEN}$  pin voltage starts to fall, and during the time until it reaches the detect voltage ( $V_{SEN} > V_{DF}$ ),

$V_{RESETB}$  is High level (=  $V_{IN}$ ).

Note: If the pull-up resistor is connected to a power supply other than the power input pin  $V_{IN}$  when using the Nch open drain output (XD6132N), High level will be the voltage of the power supply to which the pull-up resistor is connected.

## OPERATIONAL DESCRIPTION (Continued)

②The  $V_{SEN}$  pin voltage continues to drop, and when it reaches the detect voltage ( $V_{SEN}=V_{DF}$ ), the Nch transistor for delay capacitance discharge turns ON, and discharge of the delay capacitance  $C_d$  starts through the delay resistor  $R_n$ .

The time from  $V_{SEN}=V_{DF}$  until  $V_{RESETB}$  reaches Low level is the detect delay time  $t_{DF}$  (the detect time when the capacitor is not connected to the  $C_d$ /MRB pin is  $t_{DF0}$ ). The delay capacitance  $C_d$  is discharged through the delay resistor  $R_n$  when it is above the threshold voltage of  $V_{TCD2}$ . When it is below the threshold voltage of  $V_{TCD2}$ , the delay capacitance  $C_d$  is discharged faster through the internal built-in low impedance switch.

③During the time that the  $V_{SEN}$  pin voltage is below the detect voltage  $V_{DF}$ , the delay capacitance  $C_d$  discharges to ground level. The  $V_{SEN}$  pin starts rising again, and during the time until it reaches the release voltage ( $V_{SEN}<V_{DF}+V_{HYS}$ ),  $V_{RESETB}$  holds Low level.

④The  $V_{SEN}$  pin voltage continues to rise, and when it reaches the release voltage ( $V_{DF}+V_{HYS}$ ), the Nch transistor for delay capacitance discharge turns OFF, and charging of the delay capacitance  $C_d$  through the delay resistor  $R_p$  starts. The delay capacitance  $C_d$  is discharged through the delay resistor  $R_p$  when it is below the threshold voltage of  $V_{TCD1}$ . When it is above the threshold voltage of  $V_{TCD1}$ , the delay capacitance  $C_d$  is discharged faster through the internal built-in low impedance switch.

⑤When the delay capacitance pin voltage reaches  $V_{TCD1}$ ,  $V_{RESETB}$  changes to High level.

The time from  $V_{SEN}=V_{DF}+V_{HYS}$  until the  $V_{RESETB}$  logic changes is the release delay time  $t_{DR}$  (the release time when the capacitor is not connected to the  $C_d$ /MRB pin is  $t_{DR0}$ ).

⑥During the time that the  $V_{SEN}$  pin voltage is higher than the detect voltage ( $V_{SEN}>V_{DF}$ ),  $V_{RESETB}$  holds High level.

The above operation description is for an Active Low detection product.

For an Active High product, reverse the logic of the reset pin.

In the factory shipping state, internal hysteresis is not added ( $V_{HYS}=V_{DF}\times 0.001V$ (TYP.)), so please add a hysteresis of 1% or more with an external resistor. For the calculation method, refer to <Hysteresis external adjustment function> below. Also please refer to "Notes on use 5&6" on page 19.

### <Hysteresis external adjustment function>

Hysteresis can be added as desired by inserting a resistor between the node to monitor and  $V_{SEN}$  pin, and between the  $V_{SEN}$  pin and HYS pin.

The calculation method for adding hysteresis by increasing only the release voltage and leaving the detect voltage unchanged is given below.

For the circuit schematic, refer to Fig. 3: Hysteresis Augmentation Circuit 1.

$$V_{DR}(H) = V_{DR}(T) \times \{1 + (RD/RE)\}$$

$$\text{Hysteresis width} = V_{DR}(H) - V_{DF}(T)$$

Example 1:  $RD=200k\Omega$ ,  $RE=200k\Omega$ ,  $V_{DF}(T)=1.000V$ ,  $V_{DR}(T)=1.001V$ .

$$V_{DR}(H) = 2.002V$$

$$\text{Hysteresis width} = 2.002 - 1.000 = 1.002V$$

The calculation method for detecting high voltage and adding hysteresis is shown below.

For the circuit schematic, refer to Fig. 4: Hysteresis Augmentation Circuit 2.

$$V_{DF}(H) = V_{DF}(T) \times \{1 + (R1/R2)\}$$

$$V_{DR}(H) = V_{DR}(T) \times \{1 + (R1/R2) + (R1/R3)\}$$

$$\text{Hysteresis width} = V_{DR}(H) - V_{DF}(H)$$

Example 2:  $R1=R3=500k\Omega$ ,  $R2=200k\Omega$ ,  $V_{DF}(T)=2.000V$ ,  $V_{DR}(T)=2.002V$ .

$$V_{DF}(H) = 7.0V$$

$$V_{DR}(H) = 9.009V$$

$$\text{Hysteresis width} = 9.009 - 7.0 = 2.009V$$

(Note 1)  $V_{DF}(H)$  is the detect voltage after external adjustment.

(Note 2)  $V_{DR}(H)$  is the release voltage after external adjustment.

(Note 3)  $V_{DR}(T)$  is the release voltage.

(Note 4)  $V_{DF}(T)$  is the detect voltage.

(Note 5) The  $R2$  resistance is in parallel with the internal  $R_{SEN}$  resistance, and thus to increase the accuracy of the detect voltage and release voltage after external adjustment, select an  $R2$  resistance that is sufficiently small with respect to the  $R_{SEN}$  resistance. For  $R_{SEN}$  resistance values, refer to SPEC TABLE (p.11).

(Note 6) If high voltage is to be detected, divide the voltage with resistors  $R1$  and  $R2$  so that  $V_{SEN}$  pin  $\leq 6V$ . The battery voltage (+B) assumes up to 12V in this case.

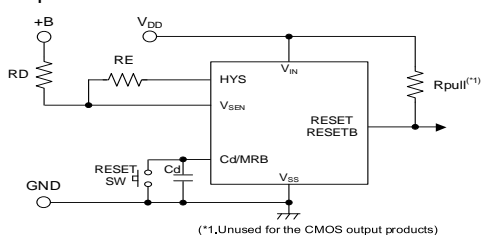


Fig. 3: Hysteresis Augmentation Circuit 1

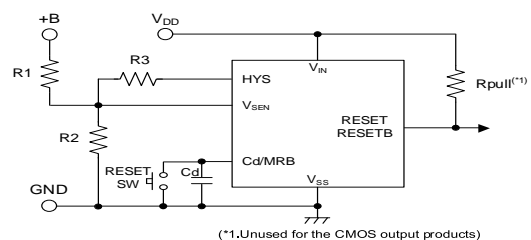


Fig. 4: Hysteresis Augmentation Circuit 2

## ■ OPERATIONAL DESCRIPTION (Continued)

### <Release delay time / detect delay time>

The release delay time and detect delay time are determined by the delay resistors ( $R_p$  and  $R_n$ ) and the delay capacitance  $C_d$ . The ratio of the delay resistances ( $R_p$  and  $R_n$ ) is selectable from 5 options. The delay time is adjustable using the combination of delay resistance and delay capacitance value. (Refer to "Selection Guide")

The release delay time ( $t_{DR}$ ) is calculated using Equation (1).

$$t_{DR} = R_p \times C_d \times \{-\ln(1 - V_{TCd1}/V_{IN})\} + t_{DR0} \dots (1) \quad * \ln \text{ is the natural logarithm.}$$

The delay capacitance pin threshold voltage is  $V_{TCd1} = V_{IN}/2$  (TYP.), and thus when

$t_{DR0}$  can be neglected, the release delay time can be calculated simply using Equation (2).

$$t_{DR} = R_p \times C_d \times \{-\ln\{1 - (V_{IN}/2)/V_{IN}\}\} = R_p \times C_d \times 0.693 \dots (2)$$

The detect delay time ( $t_{DF}$ ) is calculated using Equation (3).

$$t_{DF} = R_n \times C_d \times \{-\ln(V_{TCd2}/V_{IN})\} + t_{DF0} \dots (3) \quad * \ln \text{ is the natural logarithm.}$$

The delay capacitance pin threshold voltage is  $V_{TCd2} = V_{IN}/2$  (TYP.), and thus when

$t_{DF0}$  can be neglected, the detect delay can be calculated simply using Equation (4).

$$t_{DF} = R_n \times C_d \times \{-\ln(V_{IN}/2)/V_{IN}\} = R_n \times C_d \times 0.693 \dots (4)$$

Example 3: When type A is selected ( $R_p : R_n = 144k\Omega : 0\Omega$ ), the delay times are as follows:

If  $C_d$  is set to  $0.1\mu F$ ,

$$t_{DR} = 144 \times 10^3 \times 0.1 \times 10^{-6} \times 0.693 = 10\text{ms}$$

$t_{DF}$  is the detect delay time ( $t_{DF0}$ ) when the delay capacitance  $C_d$  is not connected.

Example 4: When type B is selected ( $R_p : R_n = 144k\Omega : 18k\Omega$ ), the delay times are as follows:

If  $C_d$  is set to  $0.1\mu F$ ,

$$t_{DR} = 144 \times 10^3 \times 0.1 \times 10^{-6} \times 0.693 = 10\text{ms}$$

$$t_{DF} = 18 \times 10^3 \times 0.1 \times 10^{-6} \times 0.693 = 1.25\text{ms}$$

(Note 7) The release delay times  $t_{DR}$  in Examples 3 and 4 are the values calculated from Equation (2).

(Note 8) The detect delay time  $t_{DF}$  in Example 4 is the value calculated from Equation (4).

(Note 9) Note that the delay times will vary depending on the actual capacitance value of the delay capacitance  $C_d$ .

### <Manual reset function>

The  $C_d$ /MRB pin can also be used as a manual reset pin.

When the  $C_d$  and RESET switch are connected to the  $C_d$ /MRB pin (refer to Fig.1), and under the release condition, if the RESET switch turns on, then the detect signal is generated at the RESET/RESETB pin forcibly.

For Active Low type (RESETB), under the release condition, if the RESET switch turns on, then the voltage at the RESETB pin changes from H to L after the detect delay time.

For Active High type (RESET), under the release condition, if the RESET switch turns on, then the voltage at the RESET pin changes from L to H after the detect delay time.

Under the detect condition, the condition will be kept even if the RESET switch turns on and off.

In the case that either H level or L level is fed to the  $C_d$ /MRB pin without the RESET switch, the behavior of the XD6132 follows the timing chart in Fig. 5.

L level is fed to the MRB pin under the detect condition, the RESET switch will be kept.

H level is fed to the MRB pin under the detect condition, the RESET switch will be undefined.

Even though the voltage at the  $V_{SEN}$  pin changes from a higher voltage than the detect voltage to a lower voltage, as long as H level is fed to the MRB pin, the release condition is kept.

If H level or L level is fed to the  $C_d$ /MRB pin forcibly, then even though  $C_d$  is connected to the pin, the XD6132 can't have any delay time.

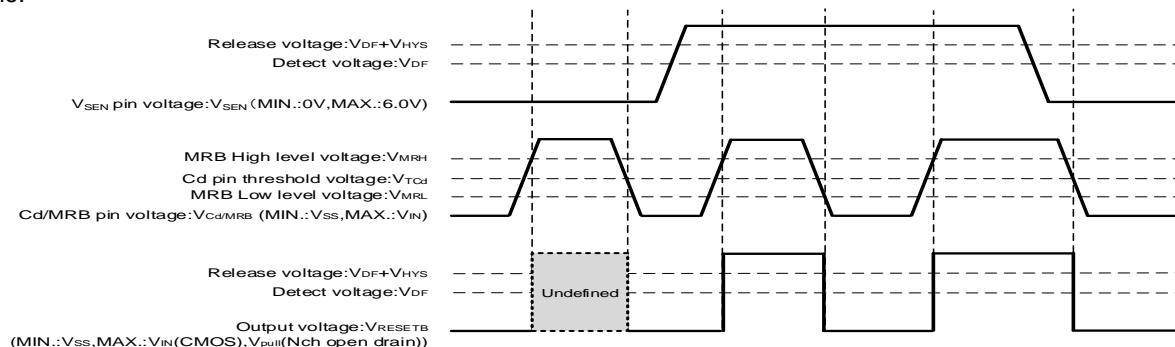


Fig. 5: Manual reset operation using the  $C_d$ /MRB pin ( $V_{IN} = 6.0V$ , Active Low product)

## OPERATIONAL DESCRIPTION (Continued)

### <Surge voltage protection function>

A surge voltage protection circuit is incorporated into the  $V_{SEN}$  pin. A surge current of  $+2.5\text{mA}(\geq 200\text{ms})$ ,  $-2.5\text{mA}(\geq 20\text{ms})$  is possible.

A positive surge current ( $I_{SENSURGE(+)}$ ) flows when M1 is turned ON by a SURGE VOLTAGE PROTECT BLOCK signal.

A negative surge current ( $I_{SENSURGE(-)}$ ) is made to flow by the M1 parasitic diode.

When a positive surge current flows and the surge voltage protection circuit activates, the  $V_{SEN}$  pin voltage rises in proportion to the  $V_{IN}$  voltage and surge current, so adjust the  $I_{SEN}$  current with an external resistor so that the  $V_{SEN}$  pin voltage does not exceed the operating voltage. Refer to Fig. 7.

※The  $V_{SEN}$  voltage rise is most pronounced at high temperature.

Example 5: When  $V_{IN}=3.3\text{V}$  and  $I_{SENSURGE(+)}=2.5\text{mA}$  (MAX), the  $V_{SEN}$  pin voltage from Fig. 7 is 5.6V. If the maximum battery voltage (+B) pin voltage is 100V, a voltage of  $(100-5.6)=94.4\text{V}$  will be applied to the R1 resistor. To keep the surge current from exceeding 2.5mA, use a resistance of  $R1=V/I=94.4/0.0025=37.8\text{k}\Omega$  or above.

Example 6: When  $V_{IN} = 3.3\text{V}$  and  $I_{SENSURGE(-)} = -2.5\text{mA}$ (MAX),  $V_f$  of the parasitic diode M1 is  $-0.9\text{V}$  (MAX).

If the battery voltage (+B) maximum is  $-100\text{V}$ , the voltage applied to the R1 resistor will be  $\{-100 - (-0.9)\} = -99.1\text{V}$ .

To limit the surge current to  $-2.5\text{mA}$ , set the R1 resistance to  $R1 = V/I = -99.1/-0.0025 = 39.6\text{k}\Omega$  or higher.

If the surge voltage on the positive side is different from the negative side, calculate the R1 resistance value using the side where the voltage difference applied to the R1 resistor is greatest.

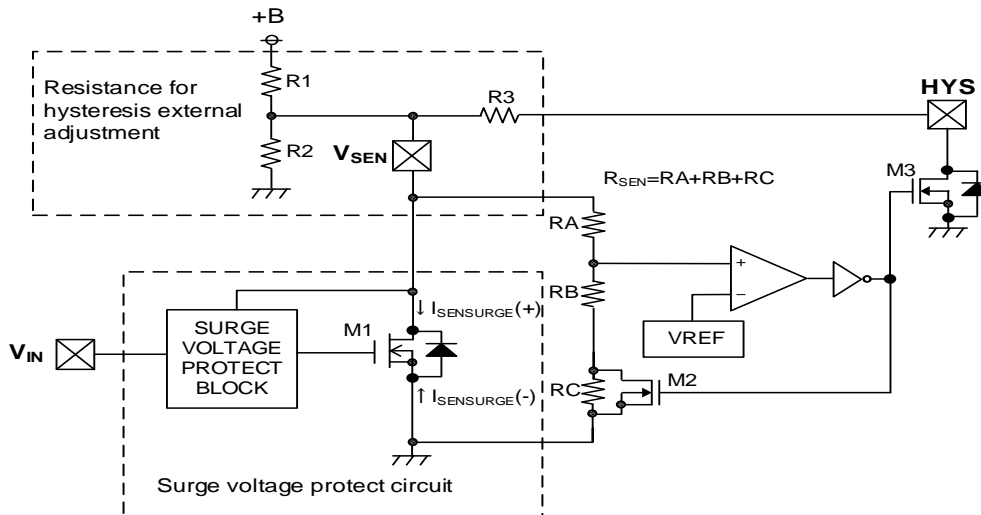


Fig. 6: Surge voltage protect circuit

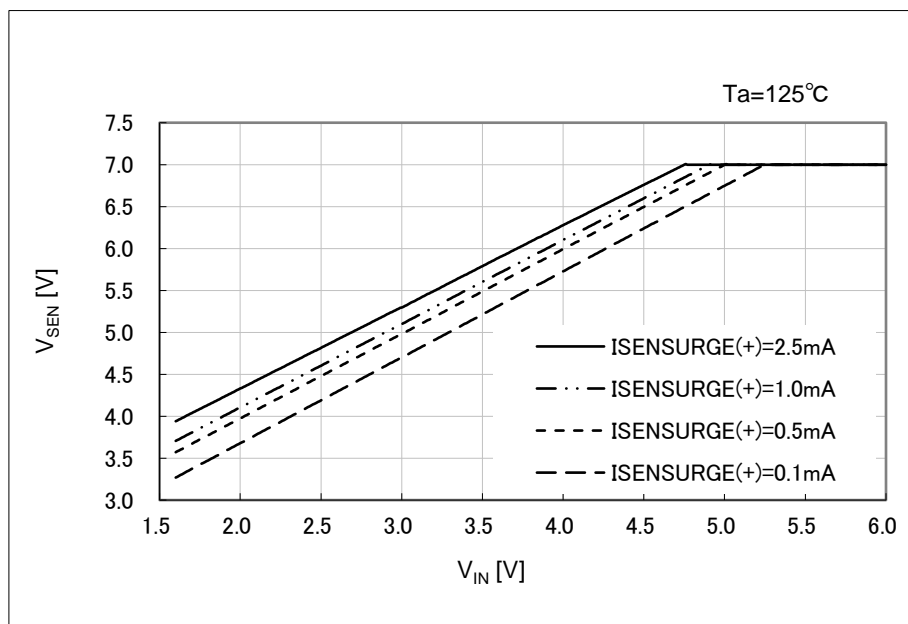


Fig. 7: Example of  $V_{IN}$ - $V_{SEN}$  characteristics



## ■ NOTES ON USE

- 1) Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
- 2) The power input pin voltage may fall due to the flow through current during IC operation and the resistance component between the power supply and the power input pin.  
In the case of CMOS output, a drop in the power input pin voltage may occur in the same way due to the output current. When this happens, if the power input pin voltage drops below the minimum operating voltage, a malfunction may occur.
- 3) Note that large, sharp changes of the power input pin voltage may lead to malfunction.
- 4) Power supply noise is sometimes a cause of malfunction. Sufficiently test using the actual device, such as inserting a capacitor between  $V_{IN}$  and GND.
- 5) Internal hysteresis is not initially included with the product. Connect external resistors to the  $V_{SEN}$  pin and HYS pin to add a hysteresis of 1% or more. Note that if hysteresis is not added with external resistors, oscillation will occur when switching takes place at the detect voltage or the release voltage.
- 6) There is a possibility that oscillation will occur if the resistances of the  $V_{SEN}$  pin and HYS pin are high. Use a resistance of 1M $\Omega$  or less between the node to monitor and  $V_{SEN}$  pin, and between the  $V_{SEN}$  pin and HYS pin.
- 7) Exercise caution if  $V_{IN}$  and  $V_{SEN}$  are started in common, as the output will be undefined until  $V_{IN}$  reaches the operating voltage.
- 8) For a manual reset function, in case when the function is activated by feeding either MRB H level or MRB L level to Cd/MRB pin instead of using a reset switch, please note these phenomena below;
  - The RESET output signal will be undefined when MRB H is fed to Cd/MRB pin under the detect condition.
  - The RESET output signal will be undefined based on the voltage relationship between  $V_{SEN}$  pin and Cd/MRB pin.
- 9) When an N-ch open drain output is used, the  $V_{RESETB}$  voltage at detection and release is determined by the pull-up resistance connected to the output pin. Refer to the following when selecting the resistance value.
 

At detection:

$$V_{RESETB} = V_{pull} / (1 + R_{pull} / R_{ON})$$

$V_{pull}$ : Voltage after pull-up  
 $R_{ON}^{(*)}$ : ON resistance of N-ch driver M6 (calculated from  $V_{RESETB} / I_{RBOUTN}$  based on electrical characteristics)

Example: When  $V_{IN} = 2.0V^{(**)}$ ,  $R_{ON} = 0.3/4.2 \times 10^{-3} = 71.4\Omega$  (MAX.).  
 If it is desired to make  $V_{RESETB}$  at detection 0.1V or less when  $V_{pull}$  is 3.0V,  
 $R_{pull} = \{(V_{pull} / V_{RESETB}) - 1\} \times R_{ON} = \{(3/0.1) - 1\} \times 71.4 \approx 2.1k\Omega$

Therefore, to make the output voltage at detection 0.1V or less under the above conditions, the pull-up resistance must be 2.1k $\Omega$  or higher.  
 (\*1) Note that  $R_{ON}$  becomes larger as  $V_{IN}$  becomes smaller.  
 (\*\*2) For  $V_{IN}$  in the calculation, use the lowest value of the input voltage range you will use.

At release:

$$V_{RESETB} = V_{pull} / (1 + R_{pull} / R_{off})$$

$V_{pull}$ : Voltage after pull-up  
 $R_{off}$ : Resistance when N-ch driver M6 is OFF (calculated from  $V_{RESETB} / I_{LEAKN}$  based on electrical characteristics)

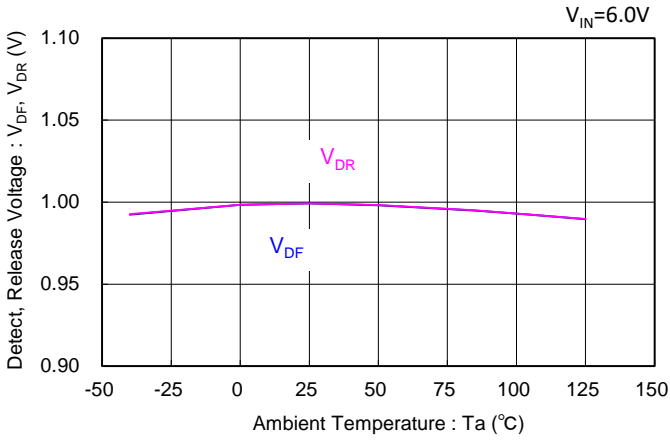
Example: When  $V_{pull}$  is 6.0V,  $R_{off} = 6 / (0.1 \times 10^{-6}) = 60M\Omega$  (MIN.). If it is desired to make  $V_{RESETB}$  5.99V or higher,  
 $R_{pull} = \{(V_{pull} / V_{RESETB}) - 1\} \times R_{off} = \{(6/5.99) - 1\} \times 60 \times 10^6 \approx 100k\Omega$

Therefore, to make the output voltage at release 5.99V or higher under the above conditions, the pull-up resistance must be 100k $\Omega$  or less.
- 10) If the discharge time of the delay capacitance Cd at detection is short and the delay capacitance Cd cannot be discharged to ground level, charging will take place at the next release operation with electric charge remaining in the delay capacitance Cd, and this may cause the release delay time to become noticeably short.
- 11) If the charging time of the delay capacitance Cd at release is short and the delay capacitance Cd cannot be charged to the  $V_{IN}$  level, the delay capacitance Cd will discharge from less than the  $V_{IN}$  level at the next detection operation, and this may cause the detect delay time to become noticeably short.
- 12) Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

## TYPICAL PERFORMANCE CHARACTERISTICS

(1) Detect, Release Voltage vs. Ambient Temperature

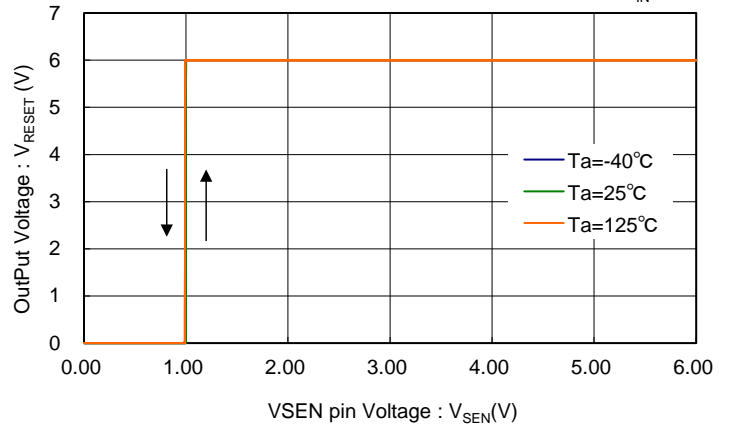
XD6132 ( $V_{DF(T)}=1.0V$ )



(2) Output Voltage vs Sense Voltage

XD6132 ( $V_{DF(T)}=1.0V$ )

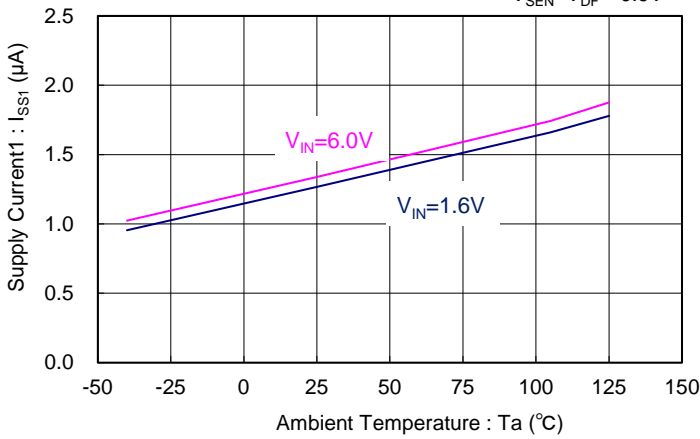
TYPE : E/F/H/K  
 $V_{IN}=6.0V$



(3) Supply Current vs. Ambient Temperature

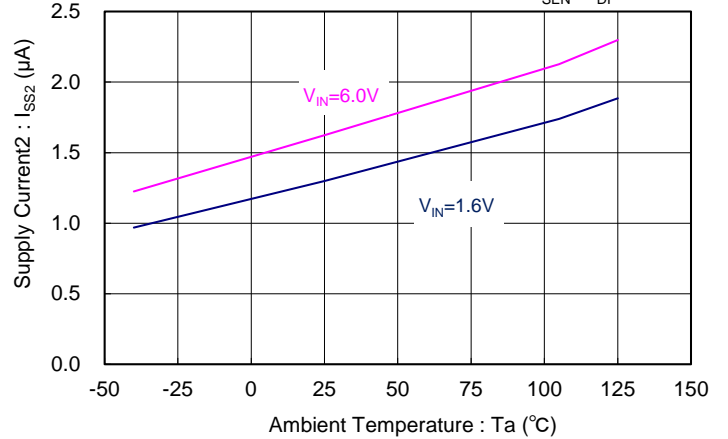
XD6132

$V_{SEN}=V_{DF} \times 0.9V$



XD6132

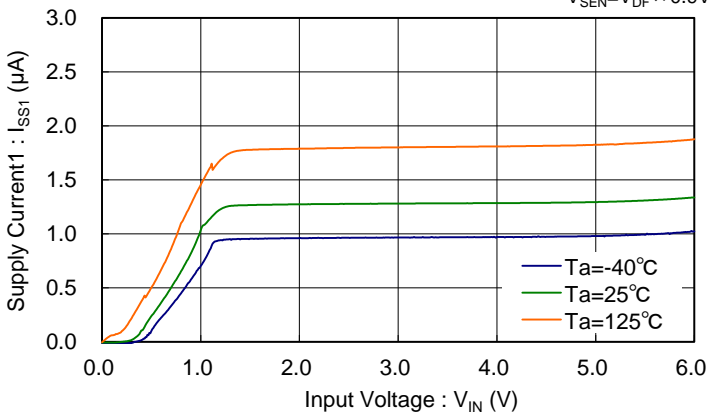
$V_{SEN}=V_{DF} \times 1.1V$



(4) Supply Current vs. Input Voltage

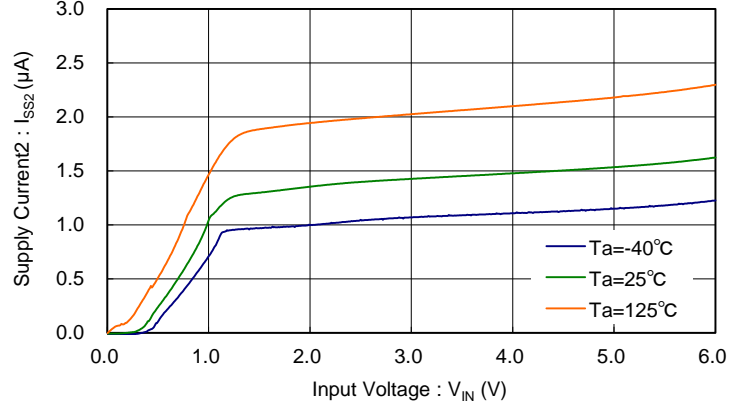
XD6132

$V_{SEN}=V_{DF} \times 0.9V$



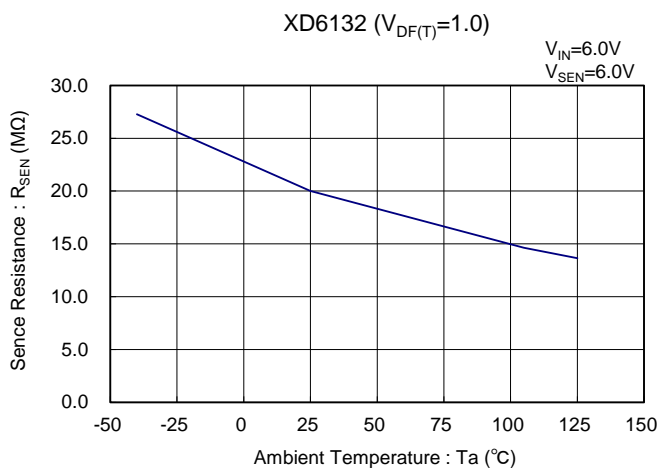
XD6132

$V_{SEN}=V_{DF} \times 1.1V$

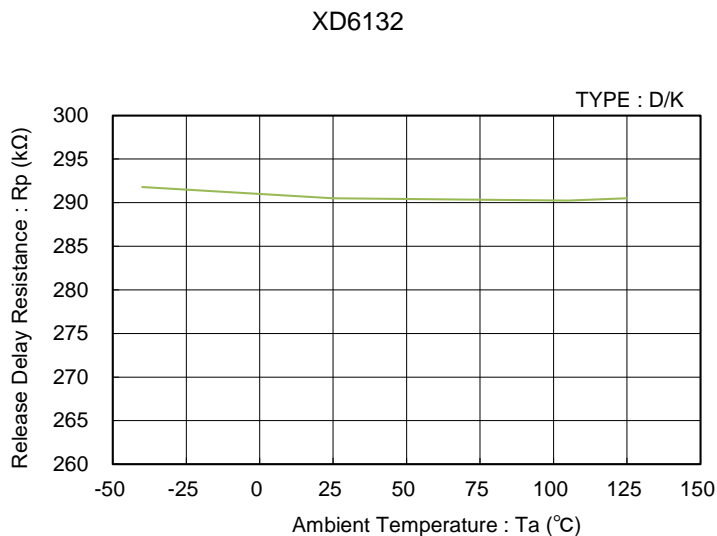
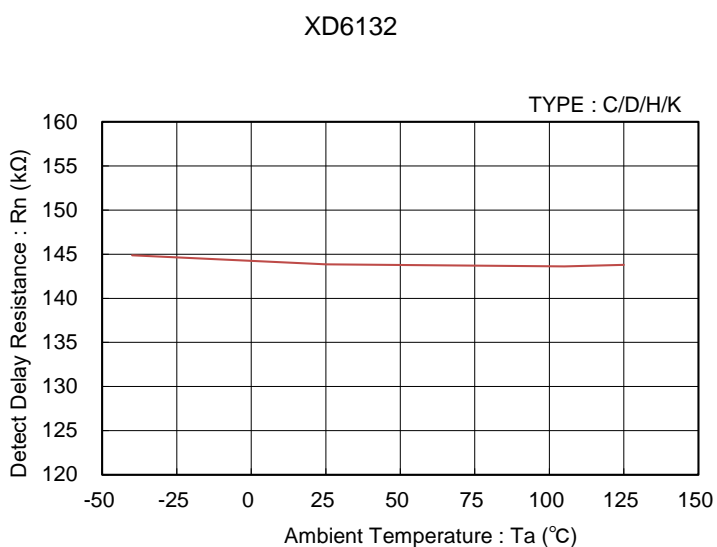
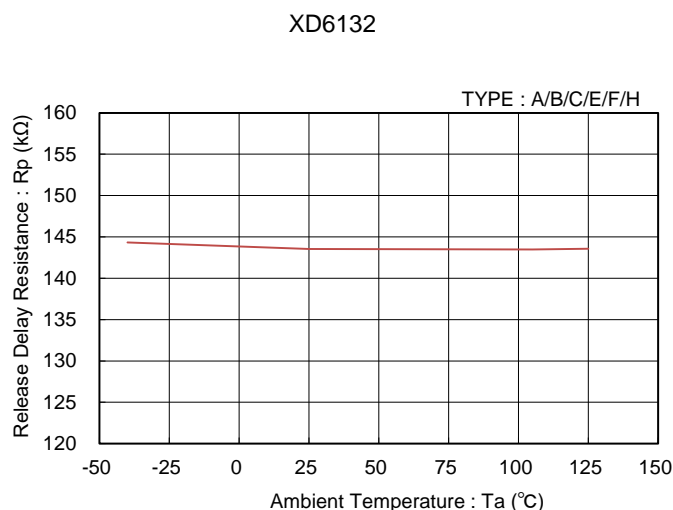
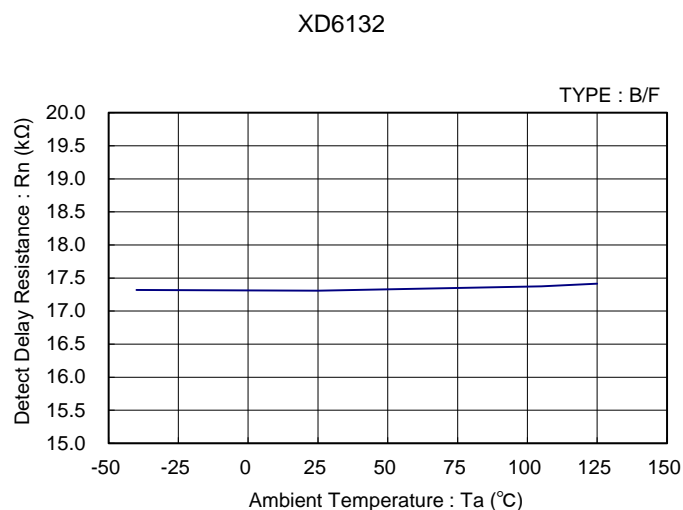


## ■ TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(5) Sense Resistance vs Ambient Temperature

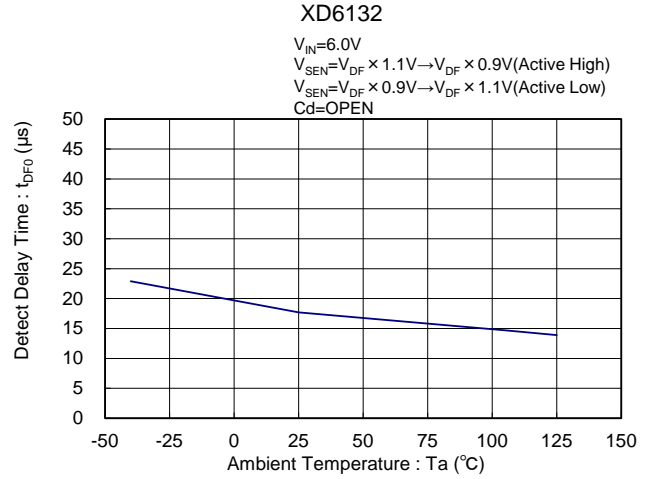
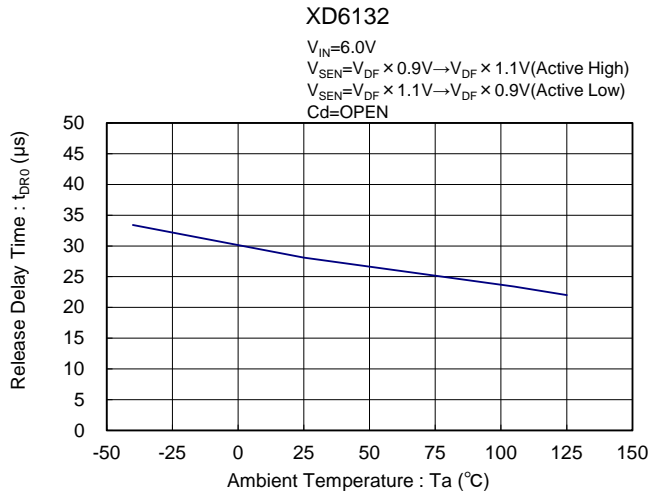


(6) Delay Resistance vs Ambient Temperature

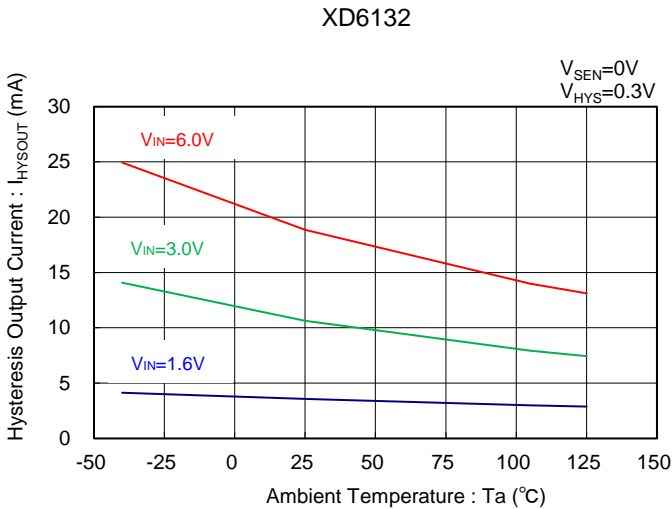


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

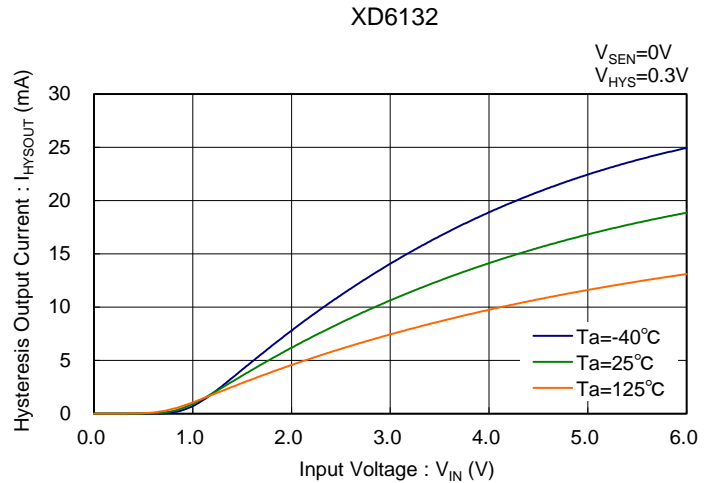
(7) Delay Time vs Ambient Temperature



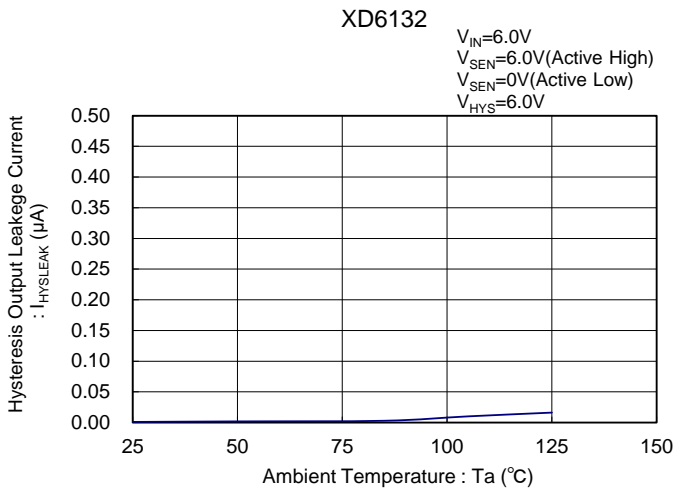
(8) Hysteresis Output Current vs Ambient Temperature



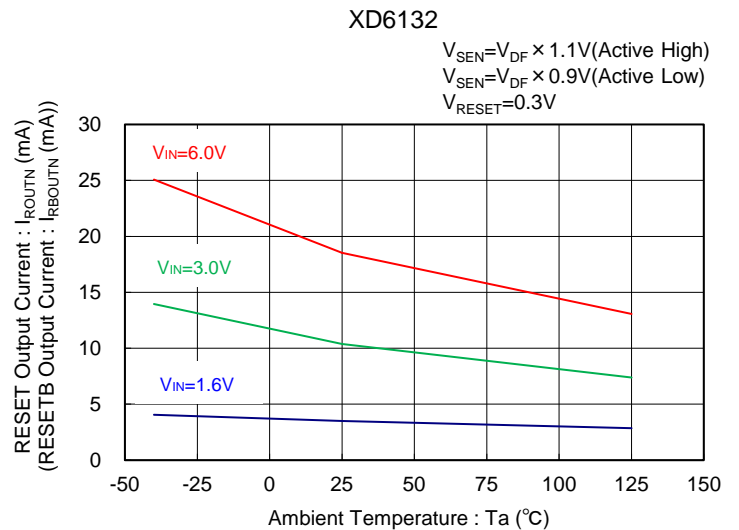
(9) Hysteresis Output Current vs Input Voltage



(10) Hysteresis Output Leakage Current vs Ambient Temperature

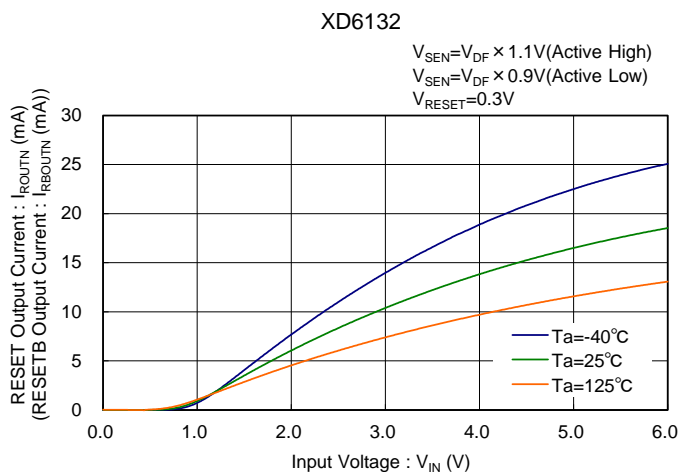


(11) RESET(RESETB) Output Current vs Ambient Temperature

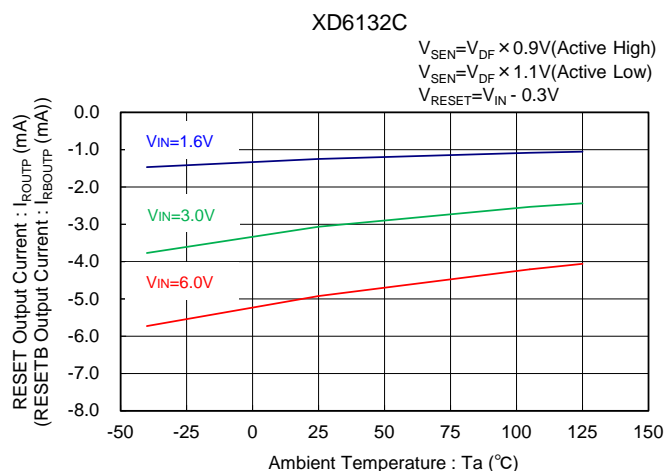


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

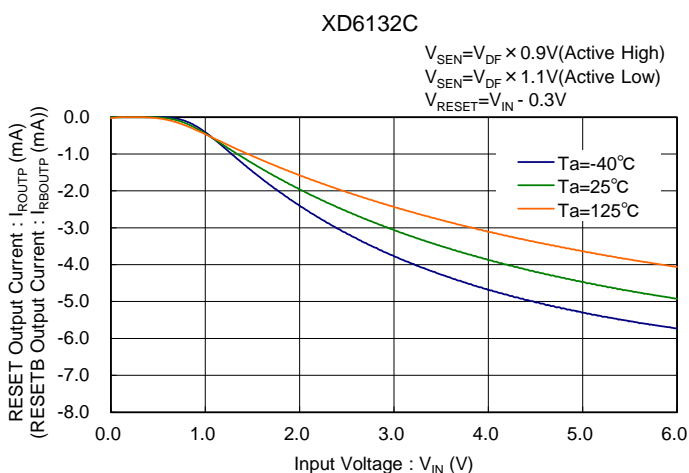
(12) RESET(RESETB) Output Current vs Input Voltage



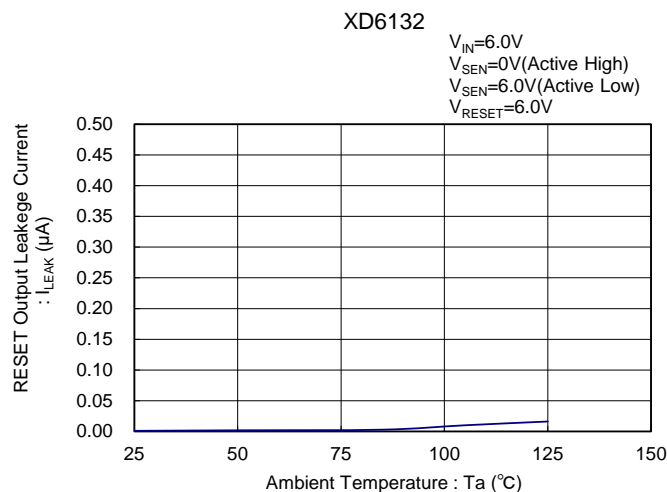
(13) RESET(RESETB) Output Current vs Ambient Temperature



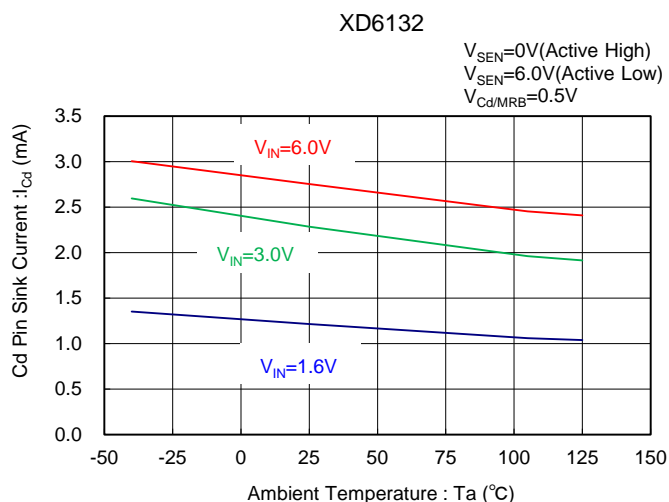
(14) RESET(RESETB) Output Current vs Input Voltage



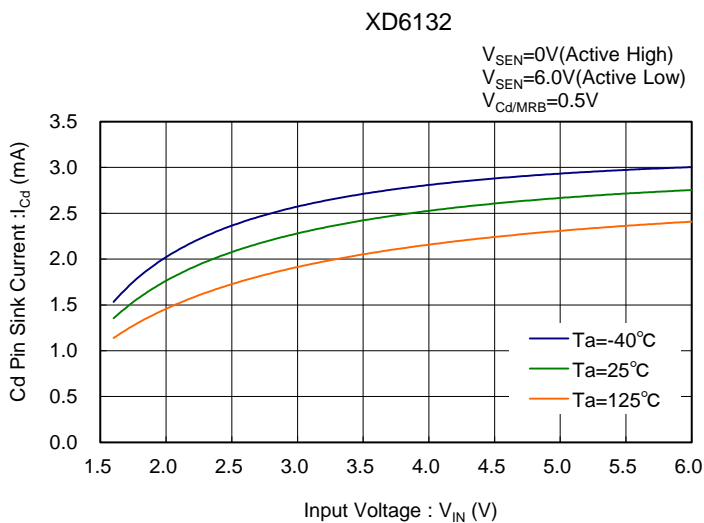
(15) RESET Output Leakage Current vs Ambient Temperature



(16) Cd Pin Sink Current vs Ambient Temperature

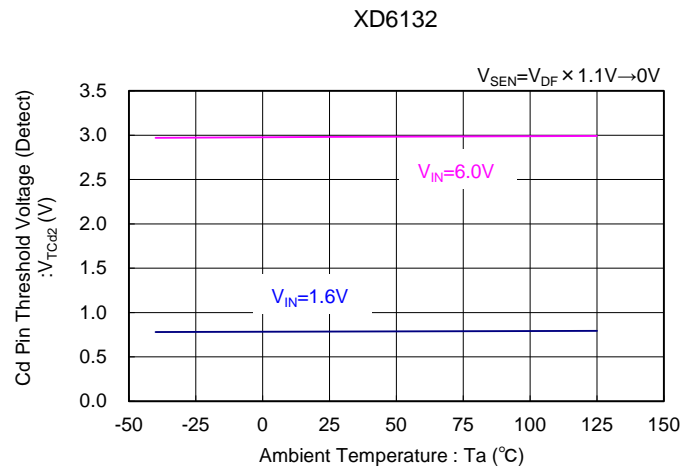
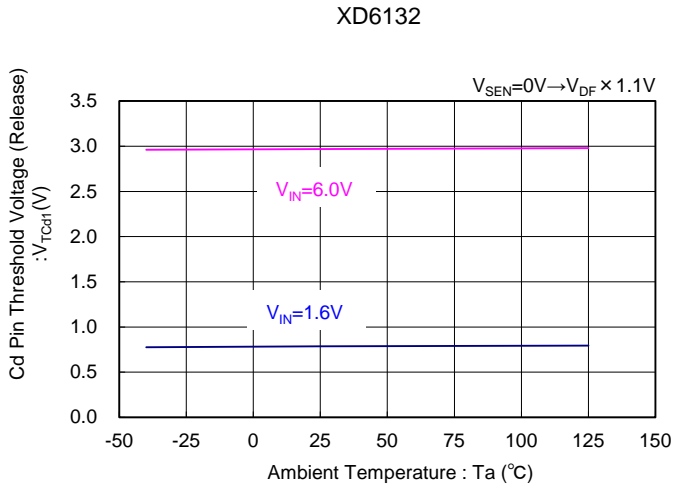


(17) Cd Pin Sink Current vs Input Voltage

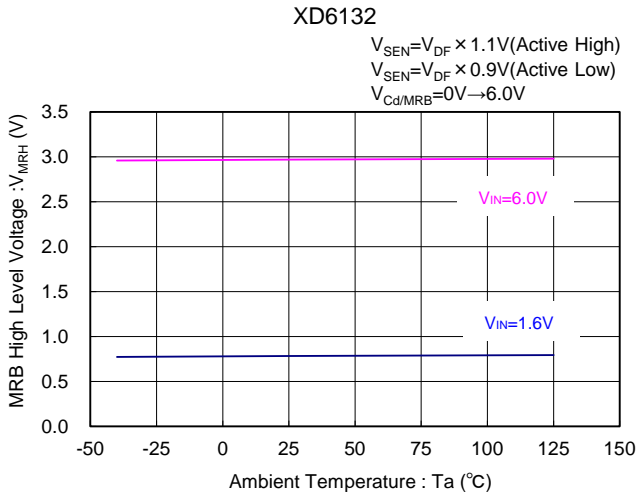


## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

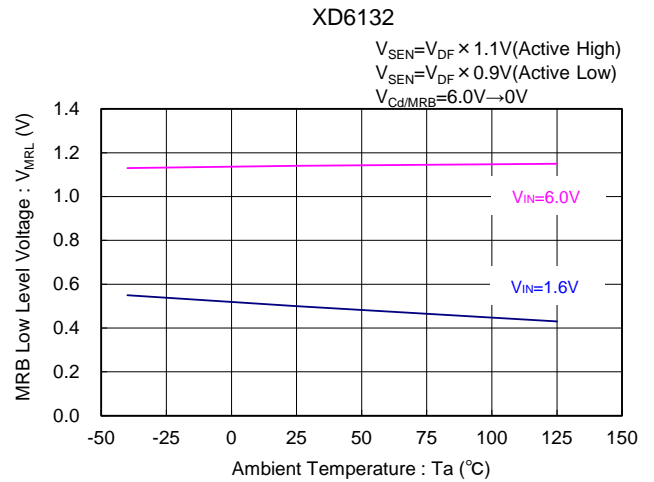
(18) Cd Pin Threshold Voltage vs Ambient Temperature



(19) MRB High Level Voltage vs Ambient Temperature



(20) MRB Low Level Voltage vs Ambient Temperature



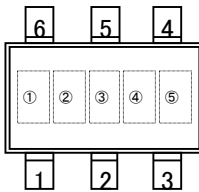
## ■ PACKAGING INFORMATION

For the latest package information go to, [www.torexsemi.com/technical-support/packages](http://www.torexsemi.com/technical-support/packages)

PACKAGE	OUTLIN / LAND PATTERN	THERMAL CHARACTERISTICS	
SOT-26	<a href="#">SOT-26 PKG</a>	Standard Board	<a href="#">SOT-26 Power Dissipation</a>
USP-6C	<a href="#">USP-6C PKG</a>	Standard Board	<a href="#">USP-6C Power Dissipation</a>
		JESD51-7 Board	

## MARKING RULE

SOT-26

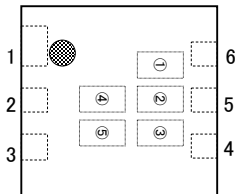


① represents products series

MARK	PRODUCT SERIES
3	XD6132*****-Q

②,③ represents internal sequential number  
 01, ...,09, 10, ..., 99, A0, ..., A9, B0, ..., B9, ..., Z9... repeated.  
 (G, I, J, O, Q, W excluded)

USP-6C



④,⑤ represents production lot number  
 01~09, 0A~0Z, 11~9Z, A1~A9, AA~AZ, B1~ZZ in order.  
 (G, I, J, O, Q, W excluded)  
 \* No character inversion used.

\*Represent product name (full product number) based on mark ①.



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