XD9263/XD9264 Series

18V Operation 500mA Synchronous Step-Down DC/DC Converters

ETR05066-001

☆AEC-Q100 Grade2

■GENERAL DESCRIPTION

The XD9263/XD9264 series are 18V operation synchronous step-down DC/DC converter ICs with a built-in high-side / low-side driver transistor. The XD9263/64 series has operating voltage range of 3V~18V and switching frequency is 2.2 MHz and it can support 500mA as an output current with high-efficiency. Compatible with Low ESR capacitors such as ceramic capacitors for the load capacitor (C_L).

0.75V reference voltage source is incorporated in the IC, and the output voltage can be set to a value from 1V to 15V using external resistors (R_{FB1}, R_{FB2}).

XD9263/XD9264 has a fixed internal soft start time which is 1.0ms (TYP.), additionally the time can be extended by using an external resistor and capacitor.

UVLO and Over current protection and thermal shutdown are embedded as protection circuits and they secure a safety operation. As an option, timer latch off overcurrent protection can be selected.

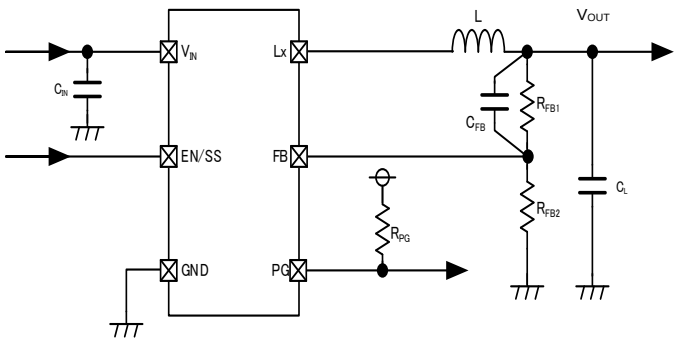
■APPLICATIONS

- ●Automotive Body Control ECU
- ●Automotive Infotainment
- ●Automotive accessories
  - ・Drive recorder
  - ・Car-mounted camera
  - ・ETC
- ●Industrial Equipment

■FEATURES

Input Voltage Range	:	3 ~ 18V (Absolute Max 20V)
FB Voltage	:	0.75V±1.5%
Oscillation Frequency	:	2.2MHz
Output Current		500mA
Quiescent Current	:	13.5μA
Control Methods	:	PWM control (XD9263) PWM/PFM Auto(XD9264) Efficiency 81%@12V→5V, 1mA
Soft-start Time	:	Adjustable by RC
Protection function	:	Over Current Protection ・Automatic Recovery (XD9263B/XD9264B) ・Integral Latch Method (XD9263A/XD9264A) UVLO Thermal Shutdown
Output Capacitor	:	Ceramic Capacitor
Operating Ambient Temperature	:	- 40℃ ~ + 105℃
Package	:	SOT-25 (No Power Good) USP-6C (With Power Good)
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

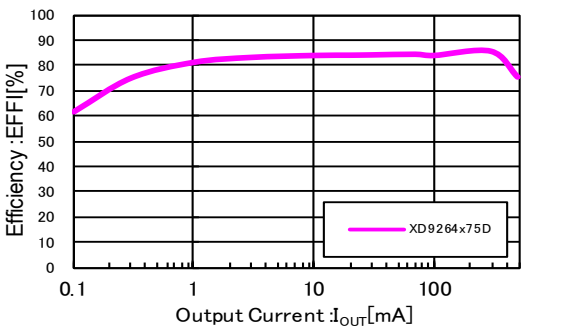


■TYPICAL PERFORMANCE CHARACTERISTICS

XD9264x75D

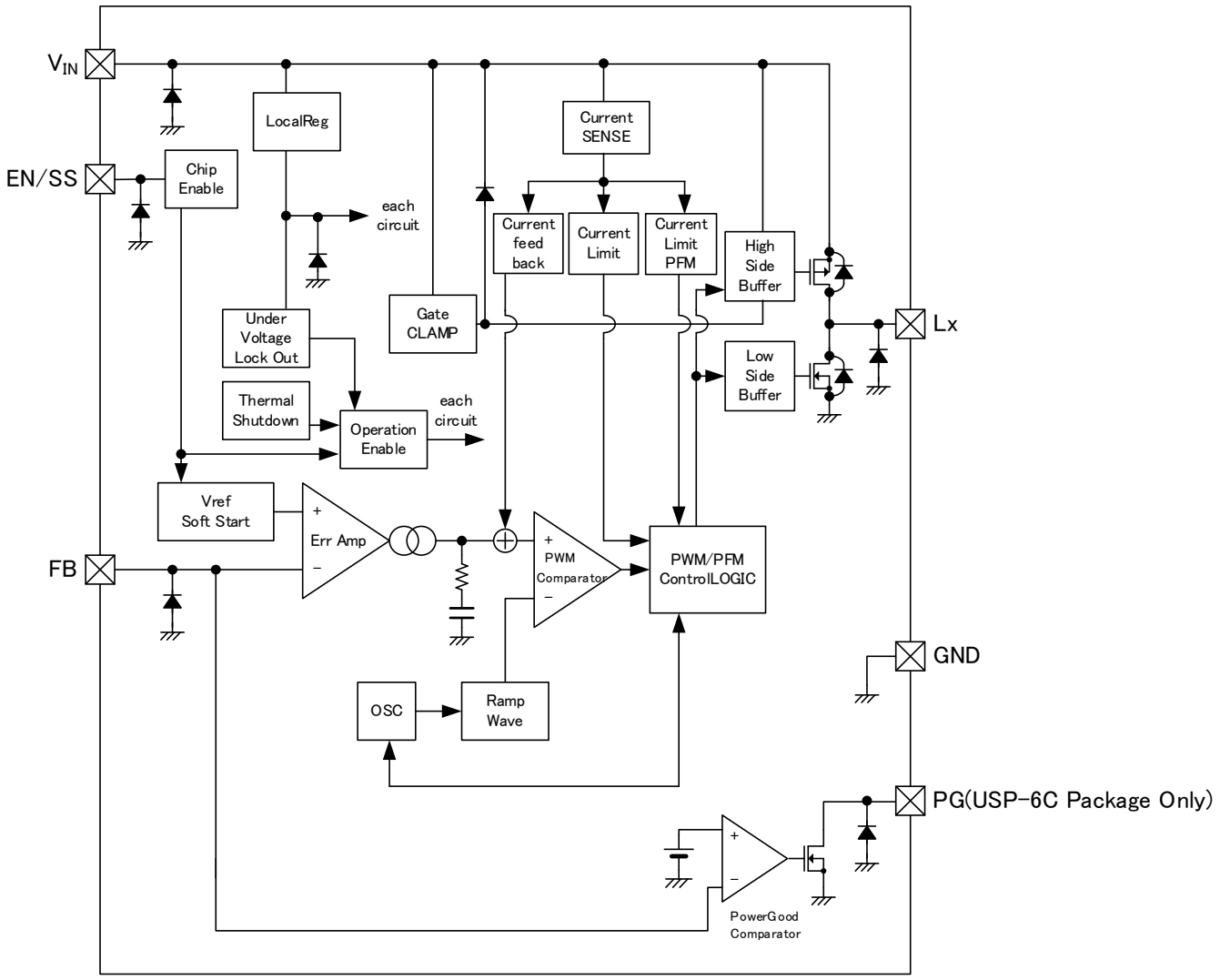
(V_{IN}=12V, V_{OUT}=5V)

L=2.2μH(CLF6045NIT-2R2), CIN=2.2μF(GRT31CC81H225KE01),
CL=10μF×2 (GRT32DC81E106KE01)



■BLOCK DIAGRAM

XD9263/ XD9264 Series



*Diodes inside the circuit are an ESD protection diodes and a parasitic diodes.

■PRODUCT CLASSIFICATION

●Ordering Information

XD9263①②③④⑤⑥-⑦(*1) PWM control

XD9264①②③④⑤⑥-⑦(*1) PWM/PFM Auto

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	A	Refer to Selection Guide
		B	
②③	FB Voltage	75	Output voltage can be adjusted in 1V to 15V
④	Oscillation Frequency	D	2.2MHz
⑤⑥-⑦	Packages (Order Unit)	MR-Q (*1)	SOT-25 (3,000pcs/Reel)
		ER-Q (*1)	USP-6C (3,000pcs/Reel)

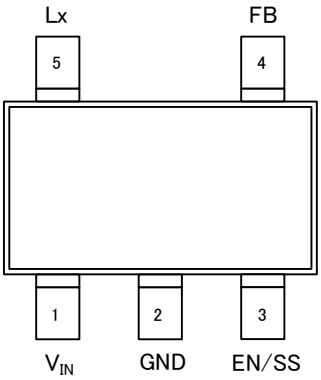
(*1) The “-Q” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

●Selection Guide

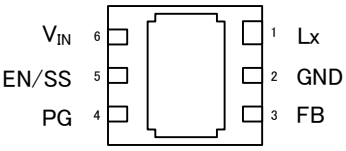
FUNCTION	A TYPE		B TYPE	
	SOT-25	USP-6C	SOT-25	USP-6C
Chip Enable	Yes	Yes	Yes	Yes
UVLO	Yes	Yes	Yes	Yes
Thermal Shutdown	Yes	Yes	Yes	Yes
Soft Start	Yes	Yes	Yes	Yes
Power-Good	-	Yes	-	Yes
Current Limitter (Automatic Recovery)	-	-	Yes	Yes
Current Limitter (Latch Protection (*2))	Yes	Yes	-	-

(*2) The over-current protection latch is an integral latch type.

■PIN CONFIGURATION



SOT-25
(TOP VIEW)



USP-6C
(BOTTOM VIEW)

* The dissipation pad for the USP-6C package should be solder-plated in recommended mount pattern and metal masking so as to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the GND (No. 2) pin.

■PIN ASSIGNMENT

PIN NUMBER		PIN NAME	FUNCTION
SOT-25	USP-6C		
1	6	V_{IN}	Power Input
3	5	EN/SS	Enable Soft-start
-	4	PG	Power-Good Output
4	3	FB	Output Voltage Sense
2	2	GND	Ground
5	1	Lx	Switching Output

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
EN/SS	L	Stand-by
	H	Active
	OPEN	Undefined State(*1)

(*1) Please do not leave the EN/SS pin open. Each should have a certain voltage.

PIN NAME	CONDITION		SIGNAL
PG	EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
		$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
		Thermal Shutdown	L (Low impedance)
		UVLO ($VIN < V_{UVLO1}$)	Undefined State
	EN/SS = L	Stand-by	L (Low impedance)

■ABSOLUTE MAXIMUM RATINGS

Ta=25℃

PARAMETER		SYMBOL	RATINGS	UNITS
V_{IN} Pin Voltage		V_{IN}	-0.3 ~ +20	V
EN/SS Pin Voltage		$V_{EN/SS}$	-0.3 ~ +20	V
FB Pin Voltage		V_{FB}	-0.3 ~ +6.2	V
PG Pin Voltage (*1)		V_{PG}	-0.3 ~ +6.2	V
PG Pin Current (*1)		I_{PG}	8	mA
Lx Pin Voltage		V_{Lx}	-0.3 ~ V_{IN}+0.3 or +20 (*2)	V
Lx Pin Current		I_{Lx}	1800	mA
Power Dissipation	SOT-25	Pd	760 (JESD51-7 Board) (*3)	mW
	USP-6C		1250 (JESD51-7 Board) (*3)	
Operating Ambient Temperature		Topr	-40 ~ +105	℃
Storage Temperature		Tstg	-55 ~ +125	℃

* All voltages are described based on the GND pin.

(*1) For the USP-6C Package only.

(*2) The maximum value should be either V_{IN}+0.3 or 20 in the lowest.

(*3) The power dissipation figure shown is PCB mounted and is for reference only.
The mounting condition is please refer to PACKAGING INFORMATION.

■ELECTRICAL CHARACTERISTICS

XD9263/XD9264 series

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
FB Voltage	V_{FB}	V_{FB}=0.731V → 0.769V V_{FB} Voltage when Lx pin voltage changes from"H" level to "L" level		0.739	0.750	0.761	V	②
			-40℃≦Ta≦105℃	0.731	0.750	0.769		
Output Voltage Setting Range(*1)	V_{OUTSET}	-	-40℃≦Ta≦105℃	1	-	15	V	−
Operating Voltage Range	V_{IN}	-	-40℃≦Ta≦105℃	3	-	18	V	−
UVLO Detect Voltage	V_{UVLO1}	V_{IN}:2.87V→2.53V、V_{FB}=0.675V V_{IN} Voltage when Lx pin voltage changes from "H" level to "L" level		2.60	2.70	2.80	V	②
			-40℃≦Ta≦105℃	2.53	-	2.87		
UVLO Release Voltage	V_{UVLO2}	V_{IN}:2.63V→2.97V、V_{FB}=0.675V V_{IN} Voltage when Lx pin voltage changes from "L" level to "H" level		2.70	2.80	2.90	V	②
			-40℃≦Ta≦105℃	2.63	-	2.97		
Quiescent Current	I_q	V_{FB}=0.825V	XD9263	-	145	234	μA	④
				-	-	239		
			XD9264	-	13.5	18.5		
				-	-	25.5		
Stand-by Current	I_{STB}	$V_{EN/SS}$=0V		-	1.65	2.5	μA	⑤
			-40℃≦Ta≦105℃	-	-	3.9		
Oscillation Frequency	f_{OSC}	Connected to external components I_{OUT}=100mA		2013	2200	2387	kHz	①
			-40℃≦Ta≦105℃	1820	-	2640		
Minimum Duty Cycle	D_{MIN}	V_{FB}=0.825V	-40℃≦Ta≦105℃	-	-	0	%	②
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.675V	-40℃≦Ta≦105℃	100	-	-	%	②
Lx SW "H" On Resistance	R_{LxH}	V_{FB}=0.675V、I_{LX}=200mA	USP-6C	-	0.95	1.10	Ω	②
			SOT-25	-	0.99	1.14		②
Lx SW "L" On Resistance	R_{LxL}	V_{FB}=0.825V、I_{LX}=200mA	USP-6C	-	0.69(*2)	-	Ω	②
			SOT-25	-	0.73(*2)	-		②
PFM Switch Current	I_{PFM}	Connected to external components、 I_{OUT}=1mA		-	370	-	mA	①
High side Current Limit (*3)	I_{LIMH}	V_{FB}=0.675V		920	1100	-	mA	②
Latch Time	t_{LAT}	Type A only Connected to external components、V_{FB}=0V		0.5	1.0	1.7	ms	⑥
Internal Soft-Start Time	t_{SS1}	$V_{EN/SS}$=0V→12V、V_{FB}=0.675V Time until Lx pin oscillates		0.5	1.0	1.7	ms	②
External Soft-Start Time	t_{SS2}	$V_{EN/SS}$=0V→12V、V_{FB}=0.675V R_{SS}=430KΩ、C_{SS}=0.47μF Time until Lx pin oscillates		17	26	35	ms	③
PG Detect Voltage(*4)	V_{PGDET}	V_{FB}=0.712V→0.638V、 R_{PG}:100kΩ pull-up to 5V V_{FB} Voltage when PG pin voltage changes from "H" level to "L" level		0.638	0.675	0.709	V	②
			-40℃≦Ta≦105℃	0.630	-	0.712		
PG Output Voltage(*4)	V_{PG}	V_{FB}=0.6V、I_{PG}=1mA	-40℃≦Ta≦105℃	-	-	0.3	V	②
Efficiency (*5)	EFFI	Connected to external components V_{OUT}=5V、I_{OUT}=1mA	XD9264	-	81	-	%	①

Test Condition: Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V

(*1): Please use within the range of V_{OUT}/V_{IN}≧0.17

(*2): Design reference value. This parameter is provided only for reference.

(*3): Current limit denotes the level of detection at peak of coil current.

(*4): For the USP-6C Package only.

(*5): EFFI = {(output voltage) x (output current)} / {(input voltage) x (input current)} x 100

■ELECTRICAL CHARACTERISTICS (Continued)

XD9263/XD9264 series

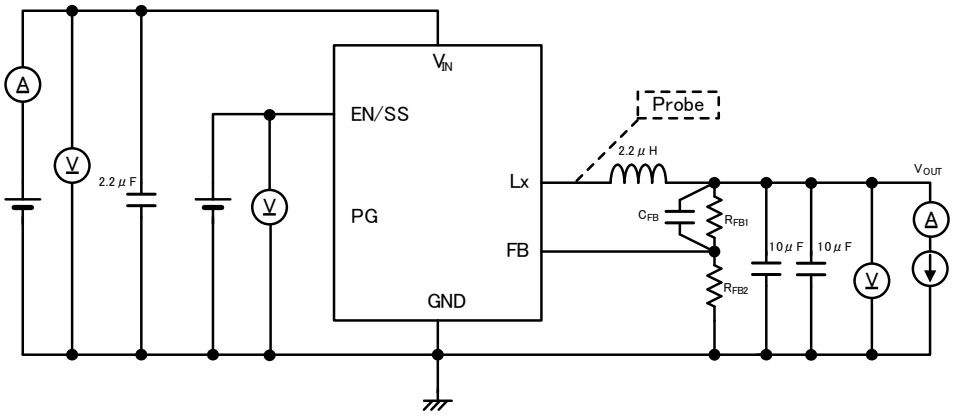
Ta=25℃

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	CIRCUIT
FB 'H' Current	I_{FBH}	V_{IN}=$V_{EN/SS}$=18V、V_{FB}=3.0V	-40℃≦Ta≦105℃	-0.1	-	0.1	μA	④
FB 'L' Current	I_{FBL}	V_{IN}=$V_{EN/SS}$=18V、V_{FB}=0V	-40℃≦Ta≦105℃	-0.1	-	0.1	μA	④
EN/SS 'H' Current	$I_{EN/SSH}$	V_{IN}=$V_{EN/SS}$=18V、V_{FB}=0.825V	-40℃≦Ta≦105℃	-	0.1	0.8	μA	④
EN/SS 'L' Current	$I_{EN/SSL}$	V_{IN}=18V、$V_{EN/SS}$=0V、V_{FB}=0.825V	-40℃≦Ta≦105℃	-0.1	-	0.1	μA	④
EN/SS 'H' Voltage	$V_{EN/SSH}$	$V_{EN/SS}$=0.3V→2.5V、V_{FB}=0.71V $V_{EN/SS}$ Voltage when Lx pin voltage changes from "L" level to "H"	-40℃≦Ta≦105℃	2.5	-	18.0	V	②
EN/SS 'L' Voltage	$V_{EN/SSL}$	$V_{EN/SS}$=2.5V→0.3V、V_{FB}=0.71V $V_{EN/SS}$ Voltage when Lx pin voltage changes from "H" level to "L"	-40℃≦Ta≦105℃	-	-	0.3	V	②
Thermal Shutdown Temperature	T_{TSD}	Junction Temperature		-	150	-	℃	-
Hysteresis Width	T_{HYS}	Junction Temperature		-	25	-	℃	-

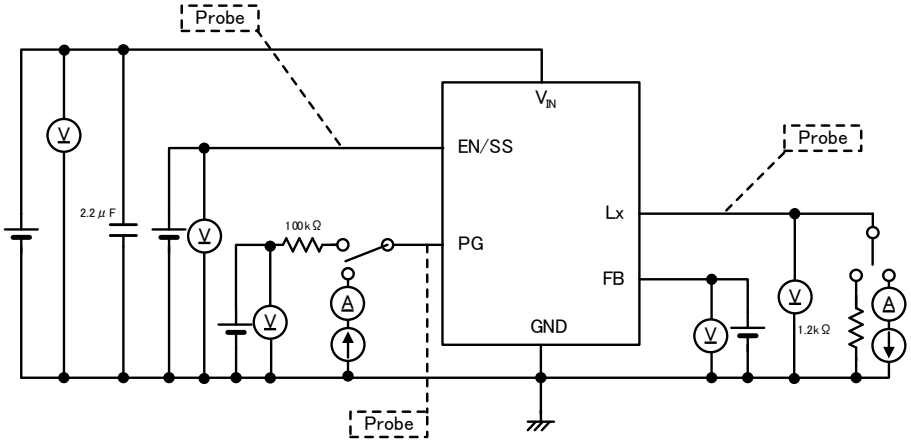
Test Condition: Unless otherwise stated, V_{IN}=12V, $V_{EN/SS}$=12V

■TEST CIRCUITS

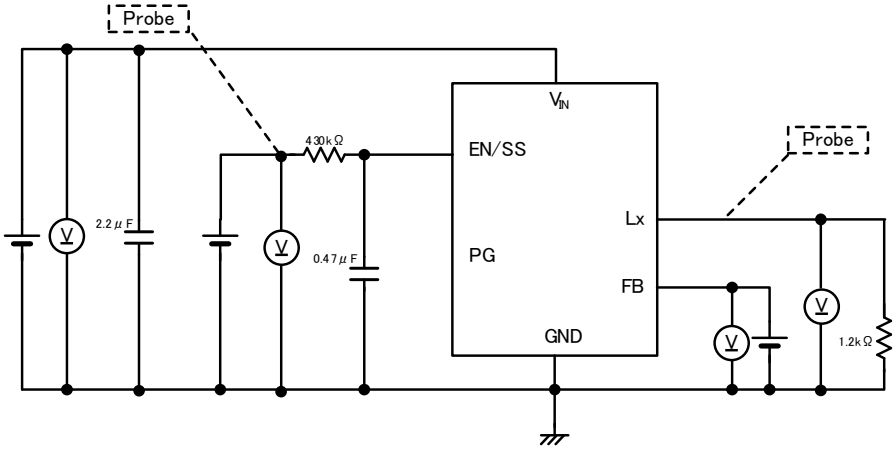
CIRCUIT①



CIRCUIT②



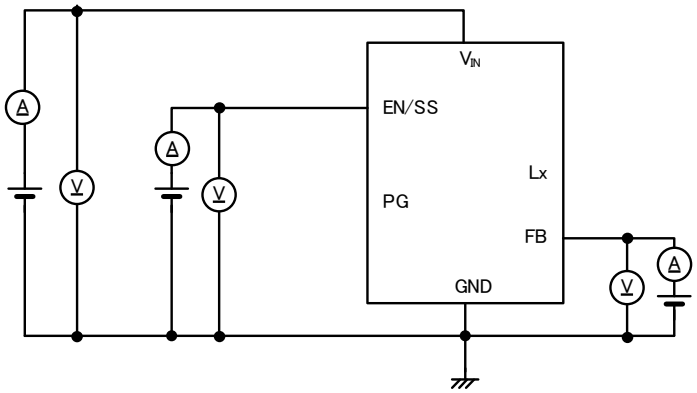
CIRCUIT③



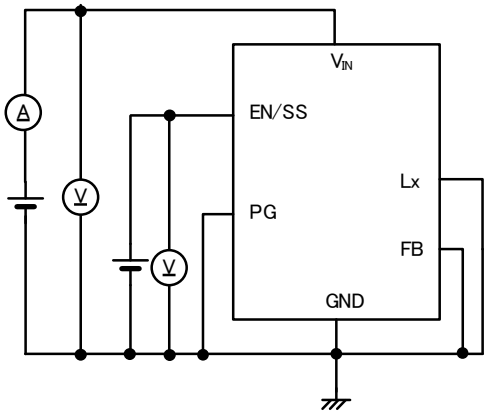
* PG Pin is USP-6C Package only.

■TEST CIRCUITS (Continued)

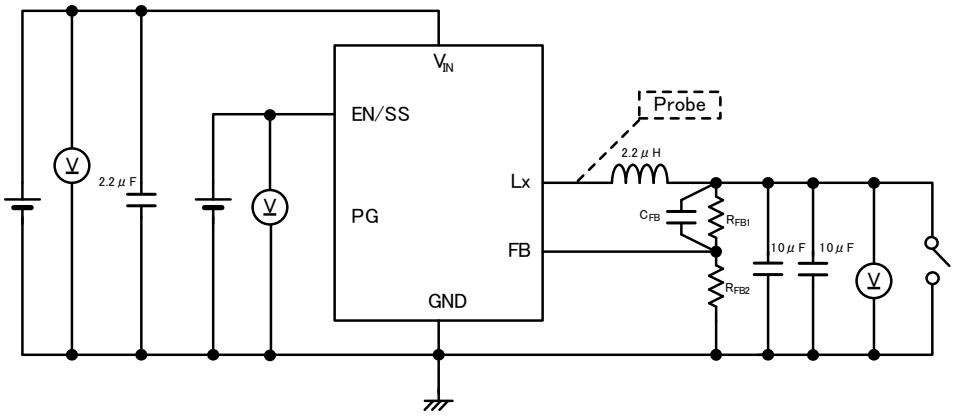
CIRCUIT④



CIRCUIT⑤

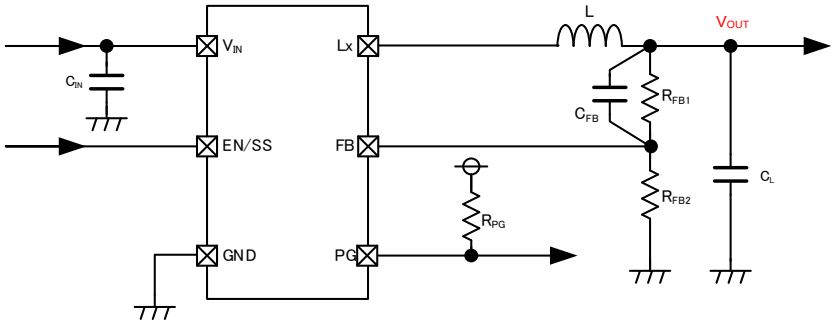


CIRCUIT⑥



* PG Pin is USP-6C Package only.

■TYPICAL APPLICATION CIRCUIT



【Typical Examples】

	MANUFACTURER	PRODUCT NUMBER	VALUE
L	TDK	CLF5030NIT-2R2N-D	2.2μH
		CLF6045NIT-2R2N-D	
	Taiyo Yuden	NRS4018T2R2MDGJV	
C_{IN}	TDK	CGA4J3X7R1E225K125AB	2.2μF/25V
	TDK	CGA4J3X7R1H225K125AB	2.2μF/50V
C_L	Murata	GRT21BR71A106KE13	10μF/10V 2parallel
	TDK	CGA5L1X7R1C106K160AC	10μF/16V 2parallel
	Murata	GRT32DC81E106KE01	10μF/25V 2parallel

<Output voltage setting>
The output voltage can be set by adding an external dividing resistor.
The output voltage is determined by the equation below based on the values of R_{FB1} and R_{FB2}.

$$V_{OUT}=V_{FB}\times(R_{FB1}+R_{FB2})/R_{FB2}$$
With $R_{FB1}+R_{FB2} \leqq 1M\Omega$

<C_{FB} setting>
Adjust the value of the phase compensation speed-up capacitor C_{FB} using the equation below.

$$C_{FB}=\frac{1}{2\pi\times fzfb\times R_{FB1}}$$

* A target value for fzfb of about 5kHz is optimum.

【Setting Example】

To set output voltage to 5V.

When R_{FB1}=680kΩ, R_{FB2}=120kΩ, V_{OUT}=0.75V×(680kΩ+120kΩ) / 120kΩ=5.0V
And fzfb is set to a target of 5kHz using the above equation,
C_{FB}=1/(2×π×5kHz×680kΩ)=46.8pF

* The setting range for the output voltage is 1.0V to 15.0V.
The condition $V_{OUT}/V_{IN} \geqq 0.17$ must be satisfied.

【Output Voltages Setting】

V_{OUT}[V]	R_{FB1}[kΩ]	R_{FB2}[kΩ]	C_{FB}[pF]
1.2	91	150	360
3.3	510	150	62
5.0	680	120	47
12	360	24	91

■TYPICAL APPLICATION CIRCUIT (Continued)

<Soft-start Time Setting>

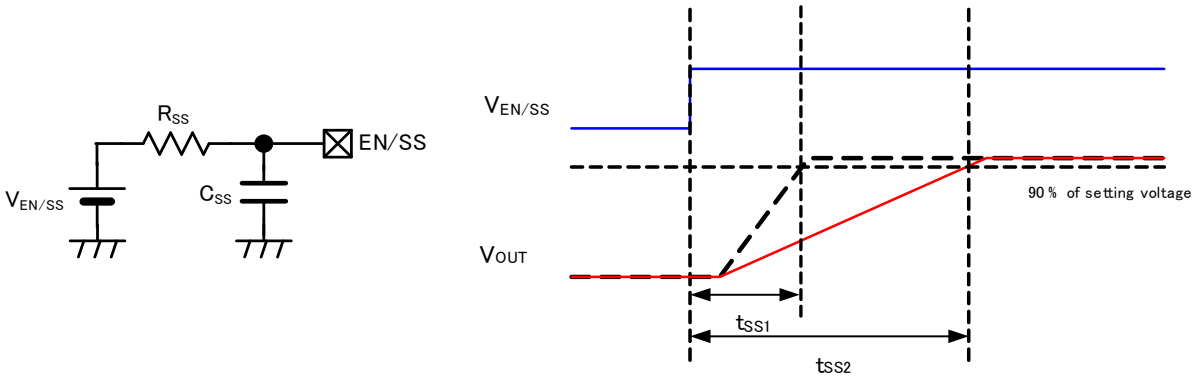
The soft-start time can be adjusted by adding a capacitor and a resistor to the EN/SS pin.
Soft-start time(t_{ss2}) is approximated by the equation below according to values of $V_{EN/SS}$, R_{SS}, and C_{SS}.

$$t_{SS2}=C_{SS}\times R_{SS}\times(-\ln((V_{EN/SS}-1.45)/V_{EN/SS}))$$

【Setting Example】

When C_{SS}=0.47μF, R_{SS}=430kΩ and $V_{EN/SS}$=12V, $t_{SS2}=0.47\times10^{-6}\times430\times10^{3}\times(-\ln((12-1.45)/12))$=26ms (Approx.)

*The soft-start time is the time from the start of $V_{EN/SS}$ until the output voltage reaches 90% of the set voltage.
If the EN/SS pin voltage rises steeply without connecting C_{SS} and R_{SS} (R_{SS}=0Ω), Output rises with taking the soft-start time of t_{ss1}=1.0ms (TYP.) which is fixed internally.



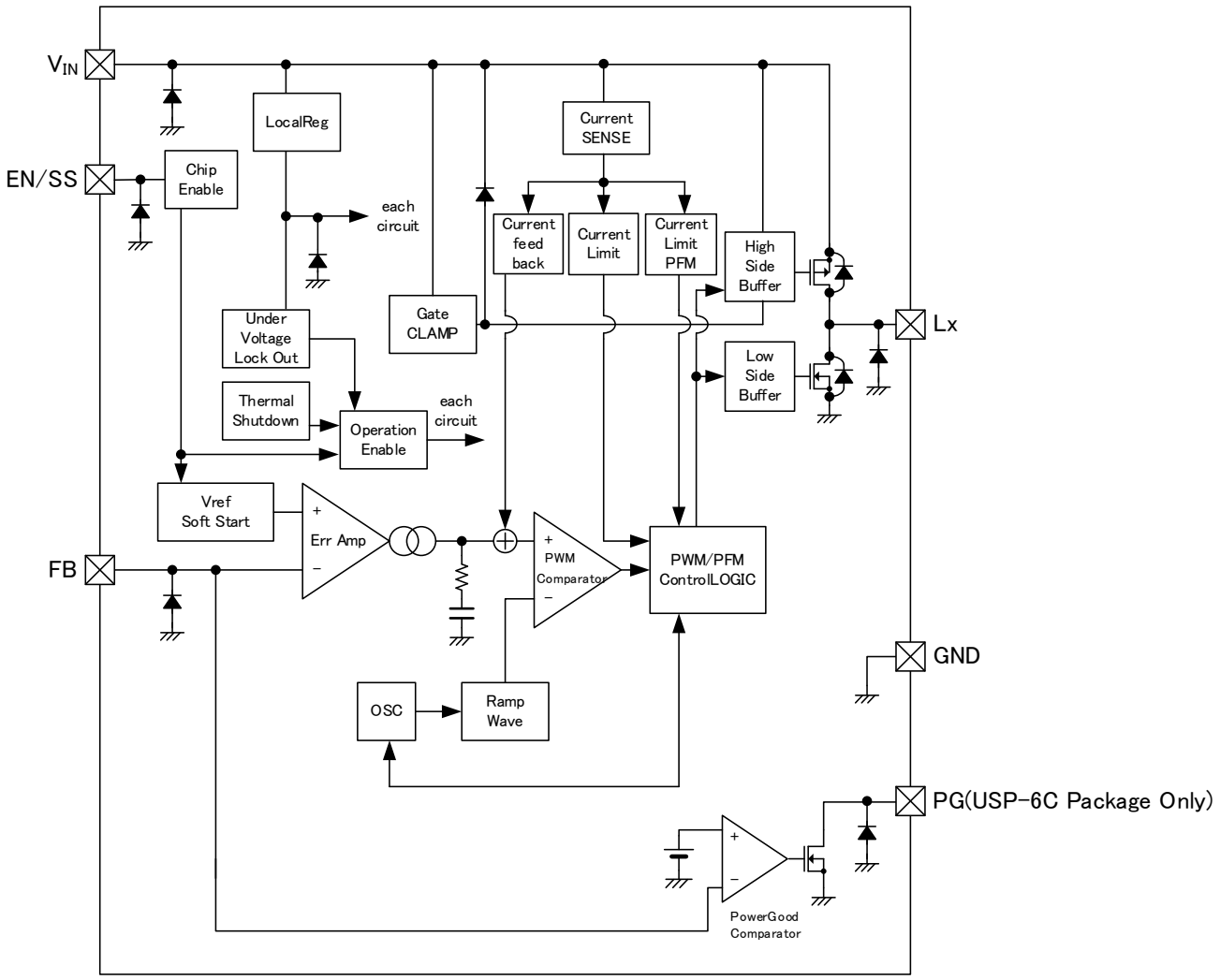
■OPERATIONAL EXPLANATION

The XD9263/XD9264 series consists internally of a reference voltage supply with soft-start function, error amp, PWM comparator, ramp wave circuit, oscillator (OSC) circuit, phase compensation (Current feedback) circuit, current limiting circuit, current limit PFM circuit, High-side driver Tr., Low-side driver Tr., buffer drive circuit, internal power supply (LocalReg) circuit, under-voltage lockout (UVLO) circuit, gate clamp (CLAMP) circuit, thermal shutdown (TSD) circuit, power good comparator, control block and other elements.

The voltage feedback from the FB pin is compared to the internal reference voltage by the error amp, the output from the error amp is phase compensated, and the signal is input to the PWM comparator to determine the ON time of switching during PWM operation. The output signal from the error amp is compared to the ramp wave by the PWM comparator, and the output is sent to the buffer drive circuit and output from the LX pin as the duty width of switching. This operation is performed continuously to stabilize the output voltage.

The driver transistor current is monitored at each switching by the phase compensation (Current feedback) circuit, and the output signal from the error amp is modulated as a multi-feedback signal. This allows a stable feedback system to be obtained even when a low ESR capacitor such as a ceramic capacitor is used, and this stabilizes the output voltage.

XD9263/ XD9264 Series



*Diodes inside the circuit are an ESD protection diodes and a parasitic diodes.

<Reference voltage source>

The reference voltage source provides the reference voltage to ensure stable output voltage of the DC/DC converter.

<Oscillator circuit>

The ramp wave circuit determines switching frequency.2.2MHz is available for the switching frequency.
Clock pulses generated in this circuit are used to produce ramp waveforms needed for PWM operation.

<Error amplifier>

The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal voltage divider, RFB1 and RFB2. When a voltage is lower than the reference voltage, then the voltage is fed back, the output voltage of the error amplifier increases. The error amplifier output is fixed internally to deliver an optimized signal to the mixer.

■OPERATIONAL EXPLANATION (Continued)

<Current limiting>

The current limiting circuit of the XD9263/XD9264 series monitors the current that flows through the High-side driver transistor and Low-side driver transistor, and when over-current is detected, the current limiting function activates.

①High-side driver Tr. current limiting

The current in the High-side driver Tr. is detected to equivalently monitor the peak value of the coil current. The High-side driver Tr. current limiting function forcibly turns off the High-side driver Tr. when the peak value of the coil current reaches the High-side driver current limit value I_{LIMH}. When the over-current state is released, normal operation resumes.

②Low-side driver Tr. current limiting

The current in the Low-side driver Tr. is detected to equivalently monitor the bottom value of the coil current. The Low-side driver Tr. current limiting function prohibits the High-side driver Tr. from turning on in an over-current state where the bottom value of the coil current is higher than the Low-side driver Tr. current limit value I_{LIML}(TYP. 0.9A). Control to lower the switching frequency f_{OSC} is also performed. When the over-current state is released, normal operation resumes.

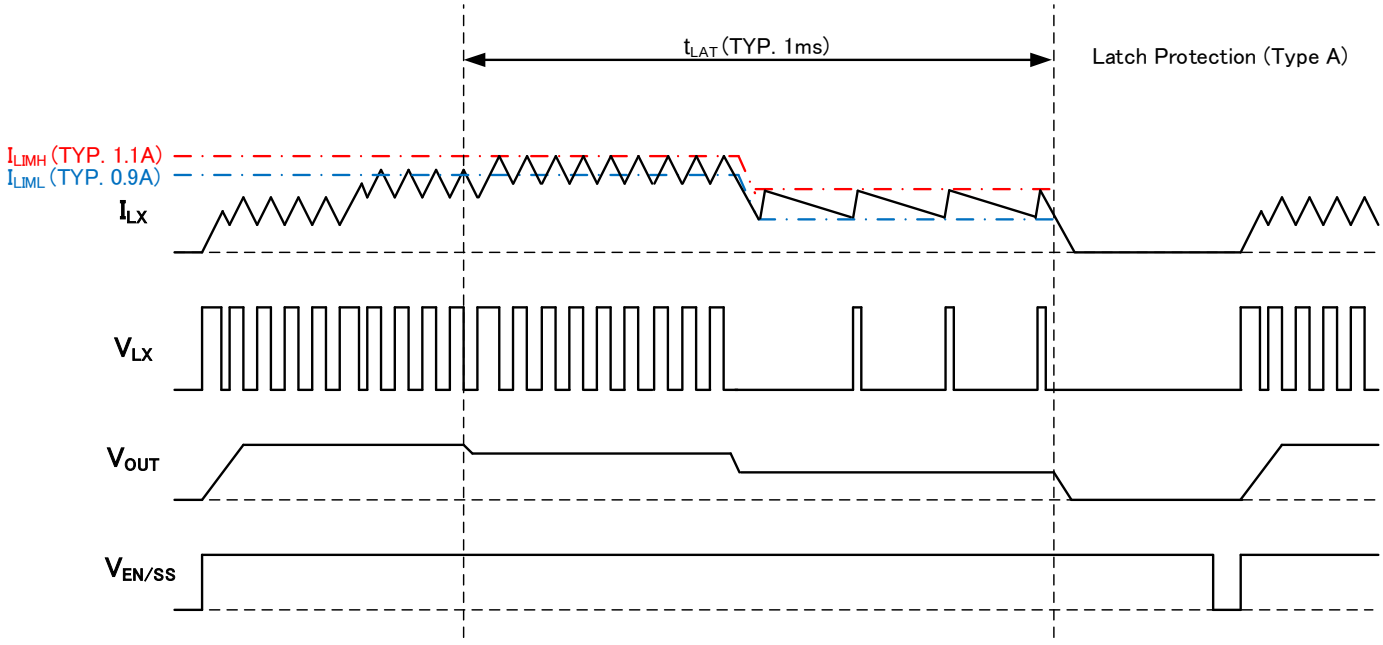
③ Over-current latch (Type A)

Type A turns off the High-side and Low-side driver Tr. when state ① or ② continues for t_{LAT} (TYP. 1.0ms). The Lx pin is latch-stopped at the GND level (0V).

The latch-stopped state only stops the pulse output from the Lx pin; the internal circuitry of the IC continues to operate. To restart after latch-stopping, L level and then H level must be input into the EN/SS pin, or VIN pin re-input must be performed (after lowering the voltage below the UVLO detection voltage) to resume operation by soft start.

The over-current latch function may occasionally be released from the current limit detection state by the effects of ambient noise, and it may also happen that the latch time becomes longer or latching does not take place due to board conditions. For this reason, place the input capacitor as close as possible to the IC.

Type B is an automatic recovery type that performs the operation of ① or ② until the over-current state is released.



Current limiting timing chart

■OPERATIONAL EXPLANATION (Continued)

<Soft-start function>

The reference voltage applied to the error amplifier is restricted by the start-up voltage of the EN/SS pin. This ensures that the error amplifier operates with its two inputs in balance, thereby preventing ON-time signal from becoming longer than necessary. Therefore, start-up time of the EN/SS pin becomes the set-time of soft-start. The soft-start time can be adjusted by adding a capacitor and a resistor to the EN/SS pin.

If the EN/SS pin voltage rises steeply without connecting C_{SS} and R_{SS} (R_{SS}=0Ω), Output rises with taking the soft-start time of t_{ss1}=1.0ms (TYP.) which is fixed internally.

The soft-start function operates when the voltage at the EN/SS pin is between 0.3V to 2.5V. If the voltage at the EN/SS pin does not start from 0V but from a middle level voltage when the power is switched on, the soft-start function will become ineffective and the possibilities of large inrush currents and ripple voltages occurring will be increased.

<Thermal shutdown>

The thermal shutdown (TSD) as an over current limit is built in the XD9263/XD9264 series.
When the junction temperature reaches the detection temperature, the driver transistor is forcibly turned off. When the junction temperature falls
to the release temperature while in the output stop state, restart takes place by soft-start.

<UVLO>

When the V_{IN} pin voltage falls below V_{UVLO1}(TYP. 2.7V), the driver transistor is forcibly turned off to prevent false pulse output due to instable operation of the internal circuits. When the V_{IN} pin voltage rises above V_{UVLO2}(TYP. 2.8V), the UVLO function is released, the soft-start function activates, and output start operation begins. Stopping by UVLO is not shutdown; only pulse output is stopped and the internal circuits continue to operate.

<Power good>

On USP-6C Package, the output state can be monitored using the power good function.

CONDITION		SIGNAL
EN/SS = H	$V_{FB} > V_{PGDET}$	H (High impedance)
	$V_{FB} \leqq V_{PGDET}$	L (Low impedance)
	Thermal Shutdown	L (Low impedance)
	UVLO ($VIN < V_{UVLO1}$)	Undefined State
EN/SS = L	Stand-by	L (Low impedance)

The PG pin is an Nch open drain output, therefore a pull-up resistance (approx. 100kΩ) must be connected to the PG pin.
When not using the power good function, connect the PG terminal to GND or use it open.

■NOTE ON USE

1) For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute MAX. specifications.

2) Make sure that the absolute maximum ratings of the external components and of this IC are not exceeded.

3) The DC/DC converter characteristics depend greatly on the externally connected components as well as on the characteristics of this IC, so refer to the specifications and standard circuit examples of each component when carefully considering which components to select.
Be especially careful of the capacitor characteristics and use B characteristics (JIS standard) or X7R, X5R (EIA standard) ceramic capacitors.
The capacitance decrease caused by the bias voltage may become remarkable depending on the external size of the capacitor.

4) If there is a large dropout voltage, then there might be pulse-skip during light loads even with PWM control.

5) The DC/DC converter of this IC uses a current-limiting circuit to monitor the coil peak current. If the potential dropout voltage is large or the load current is large, the peak current will increase, which makes it easier for current limitation to be applied which in turn could cause the operation to become unstable. When the peak current becomes large, adjust the coil inductance and sufficiently check the operation.

The following formula is used to show the peak current.

Peak Current: $Ipk = (V_{IN} – V_{OUT}) \times OnDuty / (2 \times L \times f_{OSC}) + I_{OUT}$

L: Coil Inductance [H]
f_{OSC}: Oscillation Frequency [Hz]
I_{OUT}: Load Current [A]

6) If there is a large dropout voltage, a circuit delay could create the ramp-up of coil current with staircase waveform exceeding the current limit.

7) The ripple voltage could be increased when switching from discontinuous conduction mode to Continuous conduction mode.
Please evaluate IC well on customer's PCB.

8) The operation of the IC becomes unstable below the minimum operating voltage.

9) If the voltage at the EN/SS Pin does not start from 0V but it is at the midpoint potential when the power is switched on, the soft start function may not work properly and it may cause the larger inrush current and bigger ripple voltages.

10) The effects of ambient noise and the state of the circuit board may cause release from the current limiting state, and the latch time may lengthen or latch operation may not take place. Please evaluate IC well on customer's PCB.

11) Instructions of pattern layouts
The operation may become unstable due to noise and/or phase lag from the output current when the wire impedance is high, please place the input capacitor(C_{IN}) and the output capacitor (C_L) as close to the IC as possible.

(1) In order to stabilize V_{IN} voltage level, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{IN} and GND pins.

(2) Please mount each external component as close to the IC as possible.

(3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.

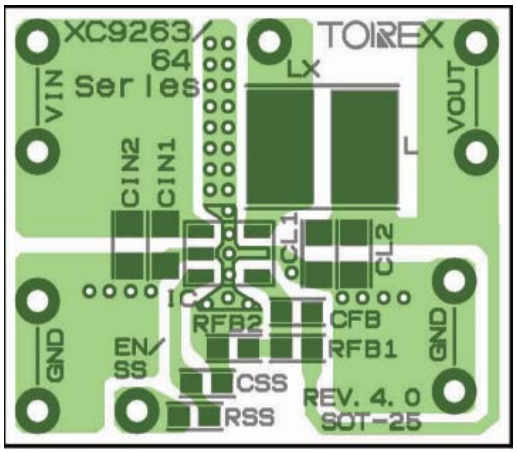
(4) Make sure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.

(5) Please note that internal driver transistors bring on heat because of the load current and ON resistance of High-side driver transistor, Low-side driver transistor

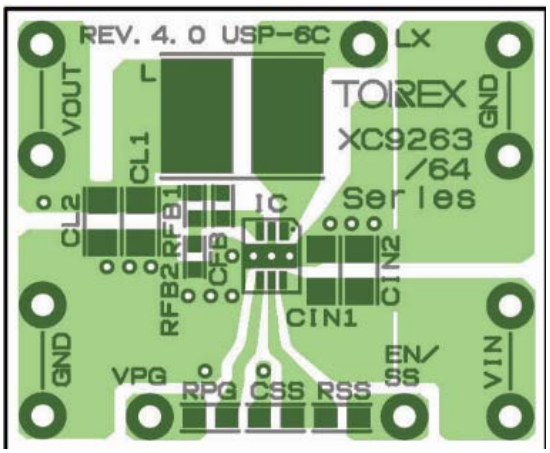
■NOTE ON USE (Continued)

<Reference Pattern Layout>

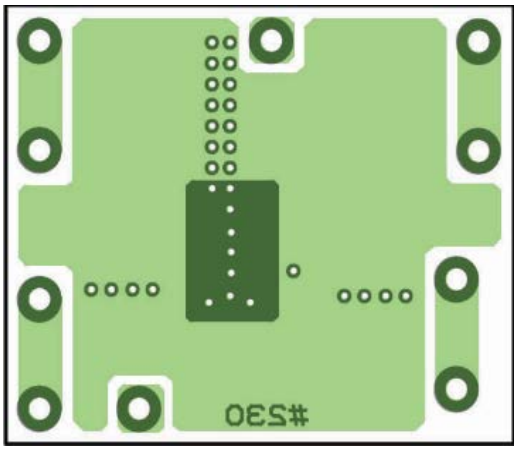
SOT-25 (Front)



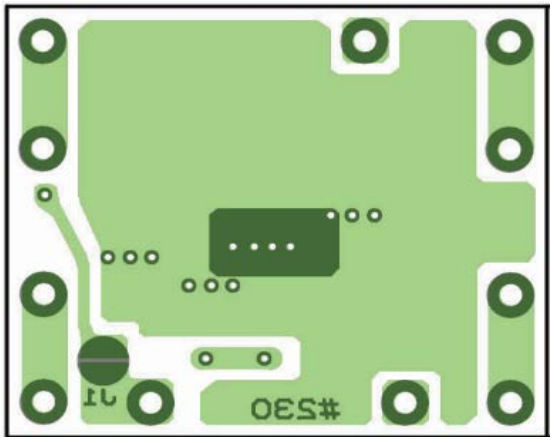
USP-6C(Front)



SOT-25(Back)



USP-6C(Back)



※XD9263/64 series PCB is the common substrate with the XC9263/64 series(non-AEC qualified products)

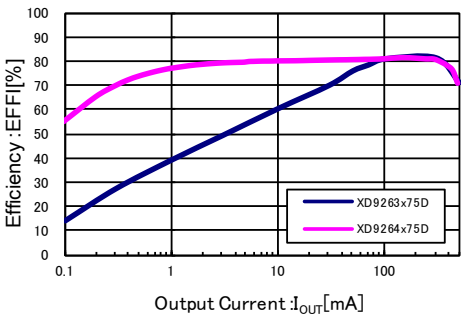
12) Torex places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using Torex products in their systems.

■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Efficiency vs. Output current

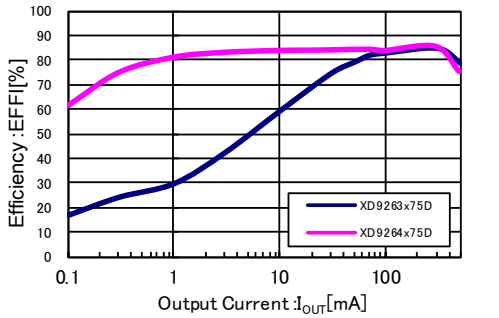
XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=3.3V)

L=2.2μH(CLF6045NIT-2R2), C_{IN}=2.2μF(GRT31CC81H225KE01),
C_L=10μF×2 (GRT32DC81E106KE01)



XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=5V)

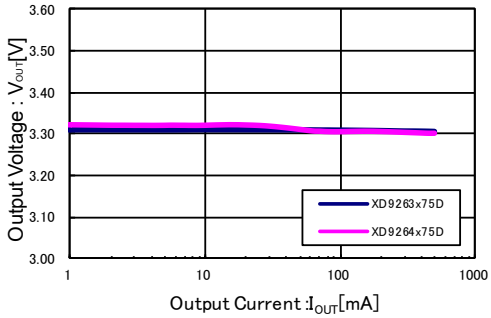
L=2.2μH(CLF6045NIT-2R2), CIN=2.2μF(GRT31CC81H225KE01),
CL=10μF×2 (GRT32DC81E106KE01)



(2) Output Voltage vs. Output Current

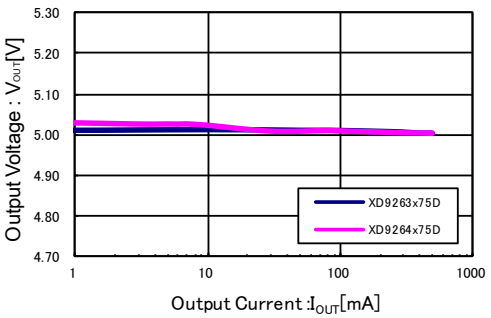
XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=3.3V)

L=2.2μH(CLF6045NIT-2R2), C_{IN}=2.2μF(GRT31CC81H225KE01),
C_L=10μF×2 (GRT32DC81E106KE01)



XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=5V)

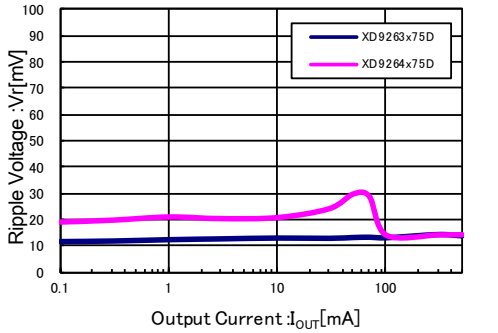
L=2.2μH(CLF6045NIT-2R2), C_{IN}=2.2μF(GRT31CC81H225KE01),
C_L=10μF×2 (GRT32DC81E106KE01)



(3) Ripple Voltage vs. Output Current

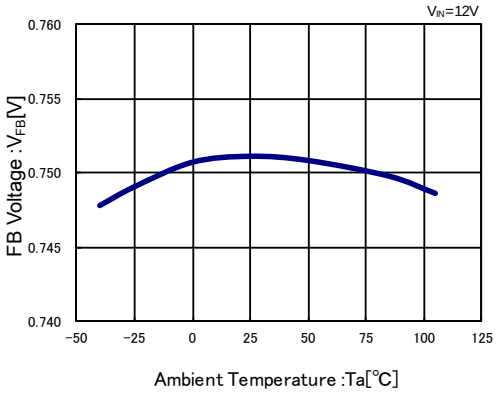
XD9263x75D/XD9264x75D
(V_{IN}=12V, V_{OUT}=5V)

L=2.2μH(CLF6045NIT-2R2), C_{IN}=2.2μF(GRT31CC81H225KE01),
C_L=10μF×2 (GRT32DC81E106KE01)



(4) FB Voltage vs. Ambient Temperature

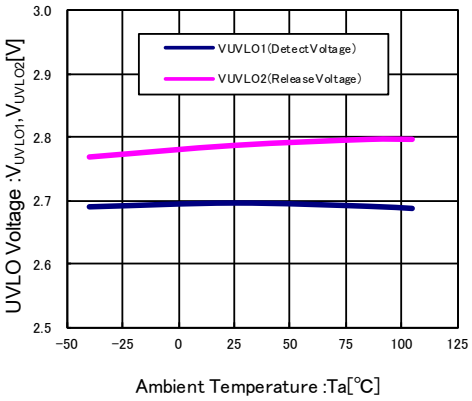
XD9263/XD9264



■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

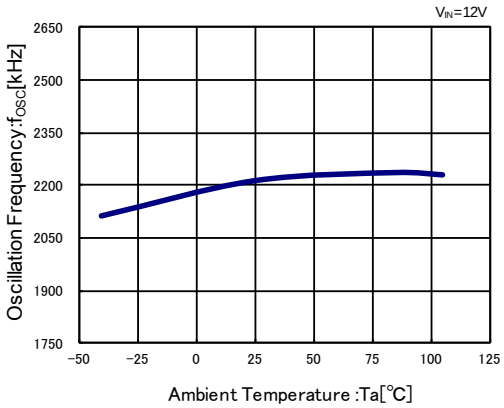
(5) UVLO Voltage vs. Ambient Temperature

XD9263/XD9264



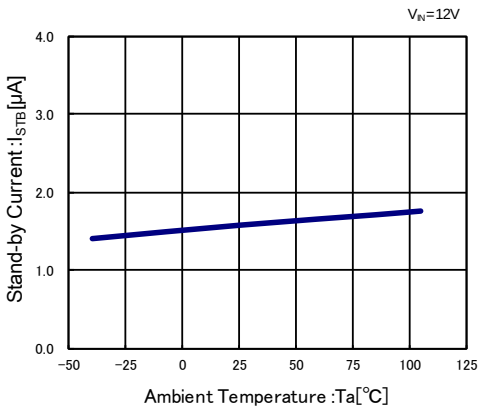
(6) Oscillation Frequency vs. Ambient Temperature

XD9263x75D/XD9264x75D



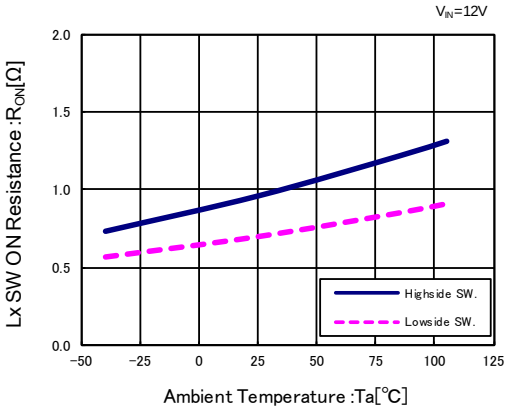
(7) Stand-by Current vs. Ambient Temperature

XD9263/XD9264



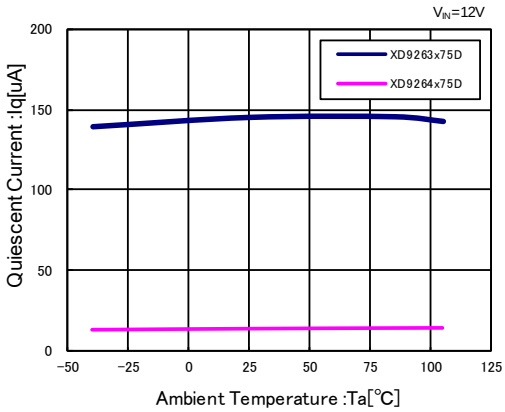
(8) Lx SW ON Resistance vs. Ambient Temperature

XD9263/XD9264



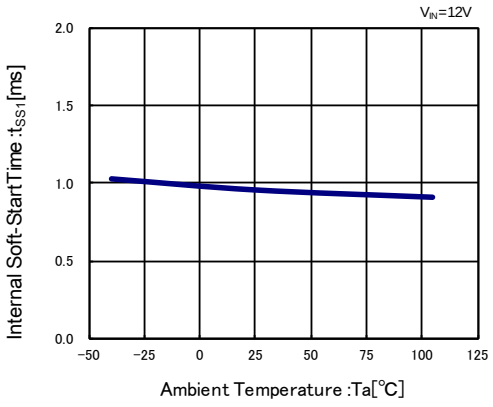
(9) Quiescent Current vs. Ambient Temperature

XD9263x75D/XD9264x75D



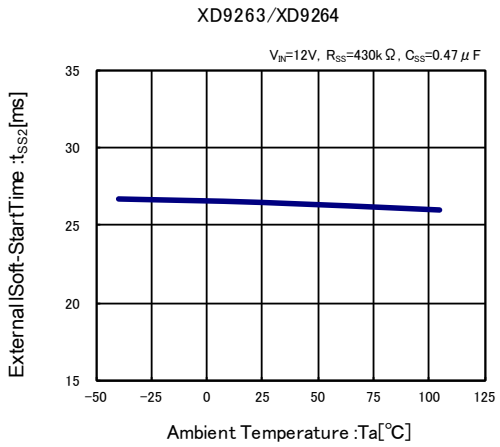
(10) Internal Soft-Start Time vs. Ambient Temperature

XD9263/XD9264

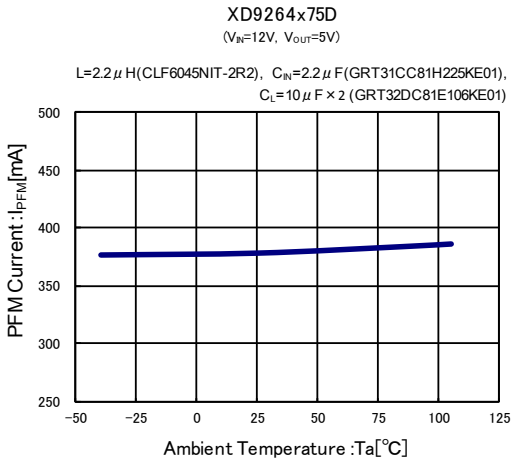


■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

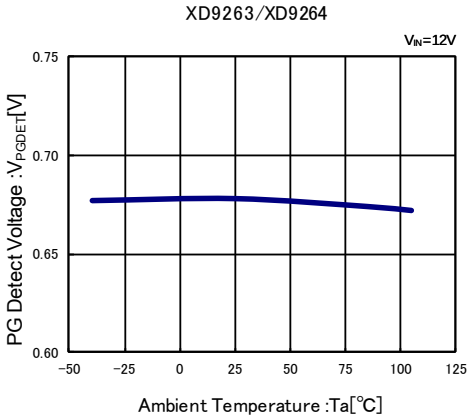
(11) External Soft-Start Time vs. Ambient Temperature



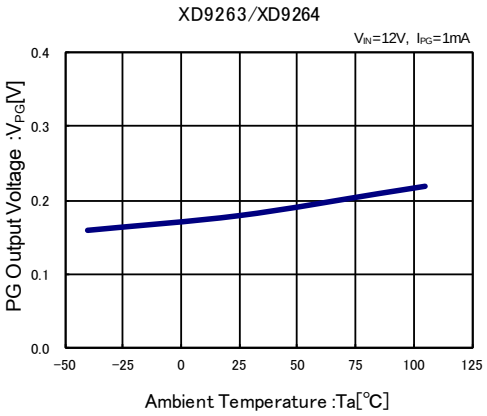
(12) PFM Current vs. Ambient Temperature



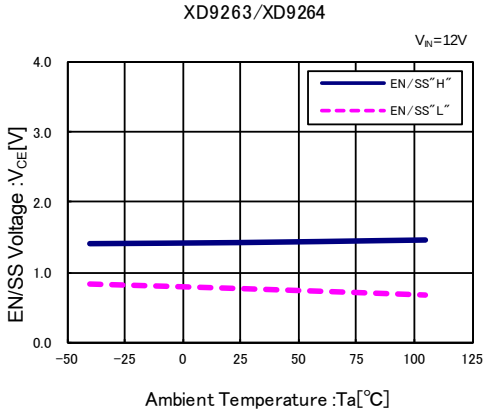
(13) PG Detect Voltage vs. Ambient Temperature



(14) PG Output Voltage vs. Ambient Temperature



(15) EN/SS Voltage vs. Ambient Temperature



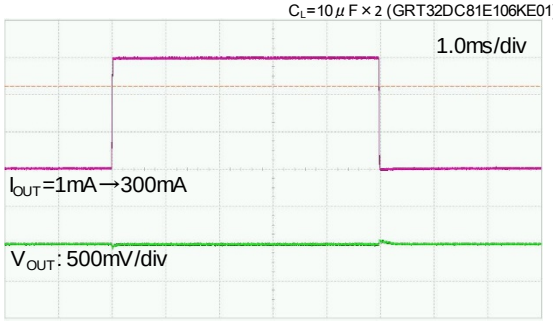
■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

(16) Load Transient Response

XD9263x75D

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=1mA→300mA

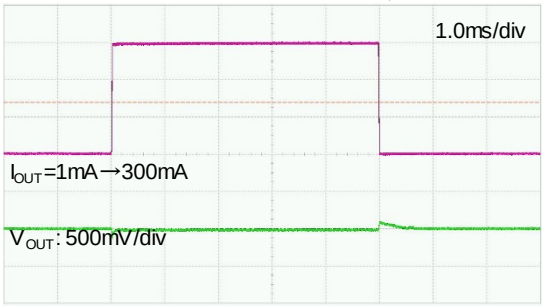
L=2.2μH(CLF6045NIT-2R2), C_{IN}=2.2μF(GRT31CC81H225KE01),
C_L=10μF×2 (GRT32DC81E106KE01)



XD9264x75D

V_{IN}=12V, V_{OUT}=5.0V, I_{OUT}=1mA→300mA

L=2.2μH(CLF6045NIT-2R2), C_{IN}=2.2μF(GRT31CC81H225KE01),
C_L=10μF×2 (GRT32DC81E106KE01)

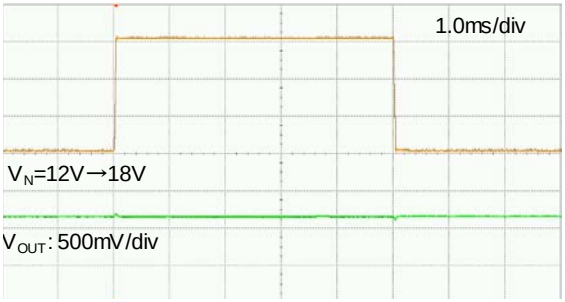


(17) Input Transient Response

XD9263x75D

V_{IN}=12V→18V, V_{OUT}=5V, I_{OUT}=300mA

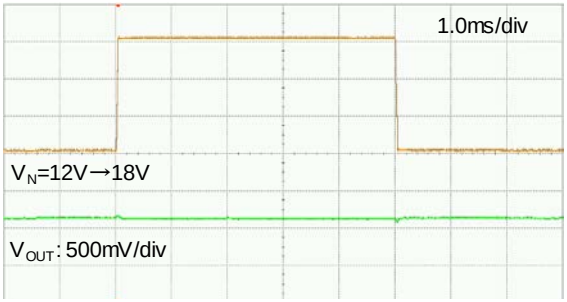
L=2.2μH(CLF6045NIT-2R2), C_{IN}=2.2μF(GRT31CC81H225KE01),
C_L=10μF×2 (GRT32DC81E106KE01)



XD9264x75D

V_{IN}=12V→18V, V_{OUT}=5V, I_{OUT}=300mA

L=2.2μH(CLF6045NIT-2R2), C_{IN}=2.2μF(GRT31CC81H225KE01),
C_L=10μF×2 (GRT32DC81E106KE01)

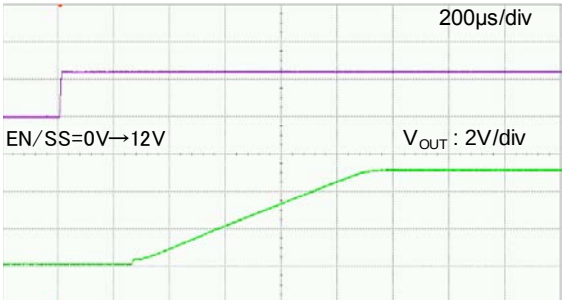


(18) EN/SS Rising Response

XD9263x75D

V_{IN}=12V, V_{CE}=0→12V, V_{OUT}=5V, I_{OUT}=300mA

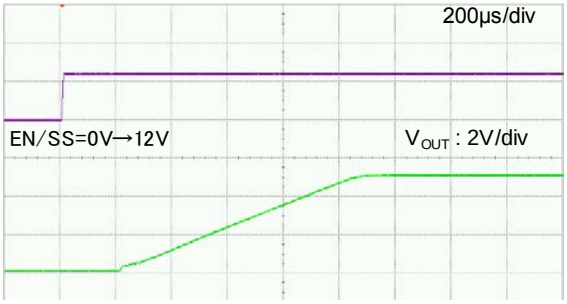
L=2.2μH(CLF6045NIT-2R2), C_{IN}=2.2μF(GRT31CC81H225KE01),
C_L=10μF×2 (GRT32DC81E106KE01)



XD9264x75D

V_{IN}=12V, V_{CE}=0→12V, V_{OUT}=5V, I_{OUT}=300mA

L=2.2μH(CLF6045NIT-2R2), C_{IN}=2.2μF(GRT31CC81H225KE01),
C_L=10μF×2 (GRT32DC81E106KE01)



■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages/

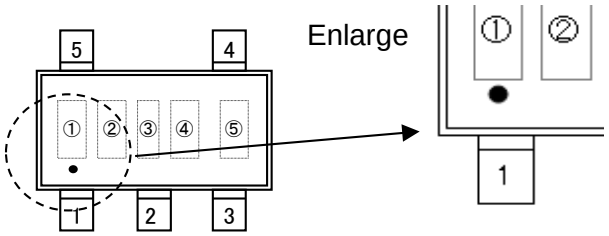
PACKAGE	OUTLIN / LAND PATTERN	THERMAL CHARACTERISTICS	
SOT-25	SOT-25 PKG	JESD51-7 Board	SOT-25 Power Dissipation
USP-6C	USP-6C PKG	JESD51-7 Board	USP-6C Power Dissipation

■MARKING RULE

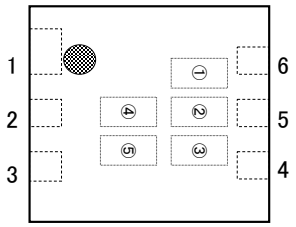
●SOT-25 / USP-6C

(*) SOT-25 has a dot mark, which is printed under MARK ① (refer to drawings below).

●SOT-25 (Under dot)



●USP-6C



①②③represents products series, products type, Oscillation Frequency

MARK			SERIES	TYPE	OSCILLATION FREQUENCY	PRODUCT SERIES
①	②	③				
L	4	1	XD9263	A	D	XD9263A75D**-Q
L	4	2	XD9263	B	D	XD9263B75D**-Q
L	4	3	XD9264	A	D	XD9264A75D**-Q
L	4	4	XD9264	B	D	XD9264B75D**-Q

④,⑤ represents production lot number
01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ, B1～ZZ in order.
(G, I, J, O, Q, W excluded)
* No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions, excluding when specified for in-vehicle use or other uses.
   Do not use the product for in-vehicle use or other uses unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

TOREX SEMICONDUCTOR LTD.